Intusoft Newsletter

Personal Computer Circuit Design Tools

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New IBIS Models From Intel

Intel's I/O Buffer Information Sheets, IBIS, are now incorporated in Intusoft digital buffer models. These new Intusoft models work with any SPICE 2G.6 compatible simulator to provide realistic predictions of circuit performance for various i486 local bus architectures, in computers using Intel's new Pentium chip, and in other application specific designs.

Ever increasing computer speeds are pushing PC board designs to the limit. Especially hard hit are mixed analog and digital circuits, requiring modeling of ground plane noise and crosstalk. With help from the Intusoft ICAPS simulation system and several new modeling developments, IsSpice simulations of all types of interconnects can play a vitally important part in insuring the success of your designs. When tackling a PCB or ASIC interconnect simulation, the problem can be broken into three modeling pieces: the transmission media, the driver, and the load. In this article, we will explore the facilities that the ICAPS simulation system provides to solve this puzzle.

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In This Issue

FilterMaster/ICAPS Combine To Create Active Filters

FilterMaster Active is the third and newest edition to the FilterMaster Design Series of filter synthesis/analysis programs. FilterMaster Active is a PC-based program used for the specification, synthesis, and analysis of active RC filters. In this article, we will develop an elliptic bandpass filter and show how easy it is to synthesis the filter circuit and then transfer the design to IsSpice for a Monte Carlo tolerance simulation.

FilterMaster Active can synthesize lowpass, highpass, bandpass, and bandstop filters. In addition to standard approximations such as Butterworth, Chebyshev, inverse Chebyshev, Elliptic, and Bessel, there are two general amplitude approximations: maximally flat and equi-ripple. These approximations have several advantages over

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New IBIS Models from Intel

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The IsSpice3 simulator has a number of elements that are useful for modeling transmission line effects. It includes 3 types of transmission lines (tlines); T, U, and O. The T element is an ideal lossless bidirectional delay line. Originally used in SPICE 2G.6, the T element has been completely reworked in IsSpice3. Highly efficient algorithms now enable IsSpice3 to simulate circuits with large numbers of tlines more than 100 times faster than SPICE 2 and with vastly improved memory efficiency. The U lossy line is based on an automatic subcircuit type expansion of a series of lumped RC segments. The capacitance of the line can also be represented with a diode capacitance characteristic. This gives the line a number of unique uses, especially when modeling interconnects within an IC.

The O element is a uniform, constant parameter, distributed line that accepts R, L, C, and G values per unit length. The parameters for the O element are inserted via a .MODEL statement. The model type is called LTRA. The operation of the LTRA model is based on the convolution of the tline's impulse responses with its inputs [1]. We will concentrate on the O element, as it can model both the T (with R=G=0) and the U (with G=L=0) lines and is usually faster and more accurate.

Lumped approximations also play an active role in tline simulations. While the tline will always give the correct answer under all rise/fall conditions, the lumped approximation may be simpler and much faster to simulate. In addition, the lumped approach allows for easy introduction of discontinuities at different points along the line. Typical interconnects, and some guidelines on which elements to use, are shown in Figures 1 and 2. The ICAPS system includes lumped models for lossless lines, ground plane coupling, and crosstalk. [3]

Many layout related problems, for example, digital switching effects on analog sections, require that tlines be coupled. To address this need, Intusoft has created a stand-alone utility,

Hierarchy of Interconnects

Types	Medium	Length	Delay
box to box	coaxial	1-10m	10-100ns
board to board	coaxial, ribbon	10cm-1m	1-10ns
chip-chip	stripline, microstrip	1-10cm	100ps-1ns
chip-pad	stripline, microstrip	1-3cm	100-300ps
intra-chip	stripline, microstrip, poly	1mm-1cm	10-100ps

Figure 1, IsSpice3 is capable of simulating all types of interconnects.

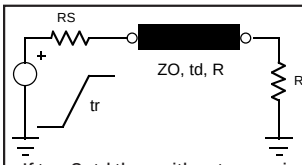


Figure 2, General guidelines for tline and lumped element selection for interconnect simulation [3,4].

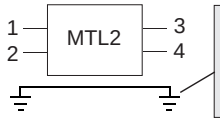
If tr < 3∗td then transmission line phenomena becomes significant.

If tr > 3∗td then either transmission line or lumped approximations can be used. The delay, td=sqrt(LC), of a single section must be < 3∗td.
If R > 5∗ZO then the line can be modeled as a distributed RC line.
If R < ZO/2 then transmission line behavior is dominant.
For multiple traces, tline effects can begin to appear when the length of the adjacent traces reach 1/10 of a wavelength (λ = v/f, v=velocity, f=frequency).

called “MULTIDEC”, to make SPICE subcircuits of multiple coupled lossy tlines. The subcircuits created by Multidec can be used with any SPICE simulator. Configurations with up to 20 coupled lossy lines can be created. The Multidec utility program is included on the *Intusoft Newsletter* floppy disk shipped to subscribers. It is important to note that the Multidec model is a simplified one. The following assumptions are made: 1) the self-inductance, self-capacitance (=ctot, not c), series resistance, parallel conductance, and capacitive/inductive coupling are the same for all lines, and 2) each line is coupled only to the two lines adjacent to it, with the same coupling parameters cm and lm. To run the Multidec program you simply call the program and state the transmission line characteristics. For example, “multidec -n2 -l9.13E-9 -c3.65E-12 -x1.8E-12 -k.482 -L2 -oTEST”, where -l is the inductance/length, -c is the capacitance/length, -x is the capacitive coupling coefficient , -k is the inductance coupling coefficient, -L is the length of the coupled line, and -o is the subcircuit name, would produce the SPICE compatible subcircuit shown in Figure 3.

Figure 3, MTL2 is a subcircuit that models a 2-conductor coupled transmission line with the parameters: l=9.13e-09, c=3.65e-12, r=0, g=0, inductive coefficient of coupling k=0.482, inter-line capacitance cm=1.8e-12, and length=10in (l, c, r, g, and cm are per inch). This gives z0 = 50Ω, td = .1825ns/in, lm=4.4n ctot=5.45p.

Subckt node convention for MTL2:



Infinite, perfect conducting, ground plane with no potential is assumed

```
∗ Lossy line models
.model mod1_MTL2 ltra rel=1.2 nocontrol r=0
+ l=4.72934e-09 g=0 c=7.25e-12 len=10
.model mod2_MTL2 ltra rel=1.2 nocontrol r=0
+ l=1.353066e-08 g=0 c=3.65e-12 len=10

.subckt MTL2 1 2 3 4
x1 1 2 5 6 m_MTL2
o1 5 0 7 0 mod1_MTL2
o2 6 0 8 0 mod2_MTL2
x2 3 4 7 8 m_MTL2
.ends MTL2

.subckt m_MTL2 1 2 3 4
v1 5 0 0v
v2 6 0 0v
f1 0 3 v1    0.707106781187
f2 0 3 v2   -0.707106781187
f3 0 4 v1    0.707106781187
f4 0 4 v2    0.707106781187
e1 7 5 3 0  0.707106781187
e2 1 7 4 0  0.707106781187
e3 8 6 3 0 -0.707106781187
e4 2 8 4 0  0.707106781187
.ends m_MTL2
```

Generic Model for Microstrip Style Interconnect

Geometric Values: 2μm thick (hth), 11μm wide (wth), 1m long (lth), and 10μm (d) above the ground. (Note: Subcircuit parameters are shown in parentheses.)
Material: aluminum - resistivity (sigma) = 2.74e-8 Ω-m
Constants: SiO2 dielectric, (er) =3.7, er0 = 8.85p MKS units, μ0 = 4e-7 ∗ π
speed of light in free space = v0 = 1/sqrt(μ0 ∗ er0) = 2.9986e8 MKS units

Line parameter calculations (per meter):
Capacitance: parallel plate
C = er ∗ er0 ∗ Area1 / d = 3.7 ∗ 8.85p ∗ 11μ ∗ 1 / 10μ = 36.02e-12 F/m
+ 30% (for fringing effects) = 46.8 pF/m

C_freespace = C0 = C/er = 46.8p/3.7 = 12.65 pF/m
v0 = 2.9986e8 = 1/sqrt(L∗C0) => L = 1/(C0 ∗ $v0^2$)
L = 1/(12.65p ∗ 8.9916e16) = 0.8792 μH/m

R = sigma ∗ lth / Area2 = 2.74e-8 ∗ 1 / (11μ ∗ 2μ) = 1245.45 Ω/m

Transmission line parameters:
Nominal z0 = sqrt(L/C) = 137Ω, td = sqrt(LC) = 6.4ns/m

```
XTMP 2 0 3 0 LLINEG {SIGMA=2.74E-8 D=10U ER=3.7
+ ER0=8.85P LTH=1 WTH=11U HTH=2U LENGTH=.16} ; 16cm line length

.SUBCKT LLINEG 1 2 3 4 {ER0=8.85P}
O1 1 2 3 4 LOSSY
.MODEL LOSSY LTRA rel=1.8 len={LENGTH}m
+ r={SIGMA*LTH/(WTH*HTH)}ohms/m g=0
+ l={1/(1.3*ER0*(LTH*WTH)/D*(2.9986E8^2))}H/m
+ c={1.3*ER*ER0*(LTH*WTH)/D}F/m
.ENDS
```

Figure 4, For microstrip lines that are very wide (w-> ∞) the line will behave like a parallel plate capacitor [5]. Equations in { } perform the line parameter calculations for any set of geometric values.

Since designers are more likely to have geometric dimensions, it is advantageous to specify the tline parameters in these terms. The example in Figure 4 shows how a generic lossy line subcircuit for a microstrip style interconnect can be set up.

Modeling The Output Driver

Modeling interconnect drive circuitry can often be a frustrating experience, especially since IC manufacturers almost never seem to give enough data to create a SPICE model. One viable method for creating IC driver models is with SpiceMod, the SPICE modeling spreadsheet program. As demonstrated in previous newsletters (Sept. '92 CMOS analog switch, Aug. '91 Dual-Gate Mosfets), SpiceMod can create very accurate IC models using existing non-proprietary data as long as a transistor level schematic is also available. The ICAPS system includes these “exact” transitor models for a variety of CMOS, TTL, and ECL gates. Several example models are included on the supplied newsletter floppy. Philips has also produced a series of exact driver models for its ALS, ABT, Mutlibyte™, FAST, Futurebus, and LVT (a 3.3V BiCMOS process) interface structures. *See The Intusoft Modeling Corner Pg. 30-12.*

Op-amp modeling has been tackled by most major hardware manufacturers. But this is not the case for most other ICs. This is due to the fact that manufacturers feel that by providing SPICE models they will, in effect, give away the store. As we have seen with Intusoft's "exact" models, this is not the case. However, Intel, along with Intusoft, have effectively side-stepped this issue with the creation of the IBIS specification.

IBIS (I/O Buffer Information Sheet) is a set of buffer operation characteristics including min and max V-I data for the output devices, diode clamp characteristics, package parasitics, and rise/fall time information [6]. By using a generic subcircuit model, also created at Intel, an end user can take IBIS data provided by a manufacturer and create a SPICE model for a particular output driver. Intel's motivation behind creating IBIS is to allow interconnect simulation by breaking down the model availability barrier and by creating a standard non-proprietary reporting format that any manufacturer can adhere to.

The buffer model put forth by Intel uses non-standard SPICE syntax based on the HSPICE® simulator. Intusoft has, therefore, made several variations with improvements to allow operation on any SPICE program. Shown in Figure 5 is the Intusoft version of the Intel generic IBIS driver. The elements B1

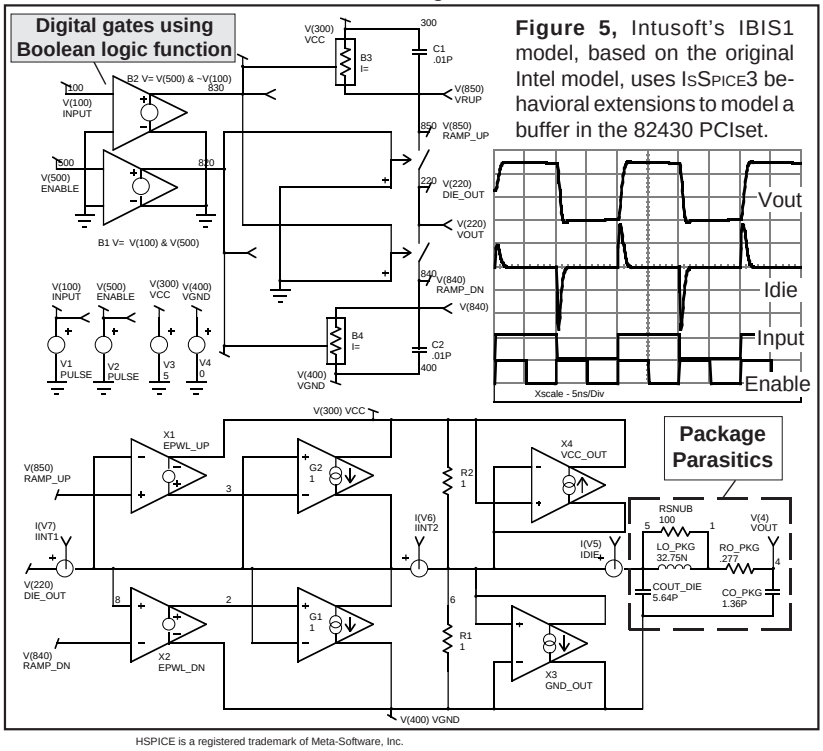


Figure 5, Intusoft's IBIS1 model, based on the original Intel model, uses IsSpice3 behavioral extensions to model a buffer in the 82430 PCIset.

HSPICE is a registered trademark of Meta-Software, Inc.

and B2 perform the tristate functions. C1 and C2, along with nonlinear resistors made using B3 and B4, account for the rise/fall time of the output signal. Intel's model uses table functions to model the pull-up/pull-down structures (X1/X2) and diode clamps (X3/X4). Note: the IBIS1 variation can only be used with IsSpice3, which supports an If-Then-Else function that is more powerful than the table model. The table model syntax used by other vendors only allows straight line segments between points. The If-Then-Else syntax is completely nonlinear, allowing virtually any transfer function between the stated points. Due to this and other modifications, the Intusoft IBIS1 model is much more streamlined than Intel's HSPICE version.

The table approach yields a generic style model that can easily be adapted and changed by the user using supplied IBIS data sheets. However, an improved model (IBIS2), using real devices (FETs/diodes) has been created. The device models are made with SpiceMod. This more true to life topology runs faster, gives more realistic results, and converges better. The main advantage of using real devices in IBIS2 is that a completely SPICE 2G.6 compatible model, that will run on any SPICE program, is created. IBIS2 is the only model version that is able to do this. The last variation, IBIS3, also uses real FETs and diodes along with digital gates and other behavioral modeling extensions found in more advanced simulators like IsSpice3.

Simulation Speed Comparison (Fig. 7)
IBIS1 (SPICE 3 compatible, Table models)
16.23s, 844 iterations
IBIS2 (SPICE 2 compatible, FETs/Diodes)
11.03s, 1144 iterations
IBIS3 (SPICE 3 compatible, FETs/Diodes)
11.8s, 1224 iterations

More data on IBIS, is available at http://www.eda.org/ibis/. As a starting point, Intusoft has created SPICE models for the 82430 PCIset of devices, using worst case and typical values, for each of the three IBIS model variations. The worst case

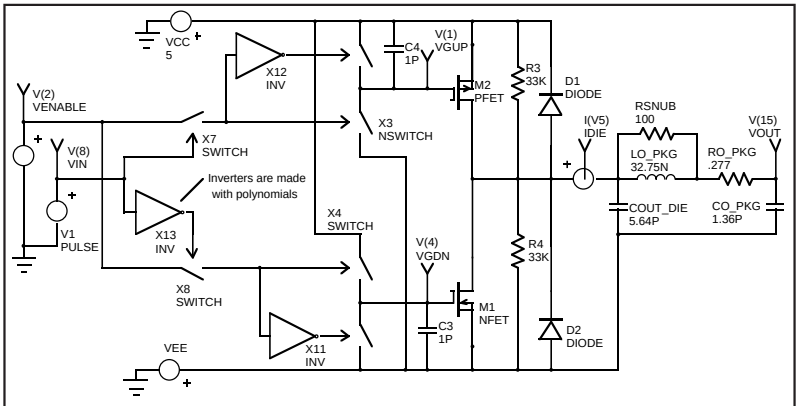


Figure 6, The Intusoft IBIS2, SPICE 2G compatible subcircuit, uses real FETs and diodes to replace the pull-up/pull-down and clamp table functions.

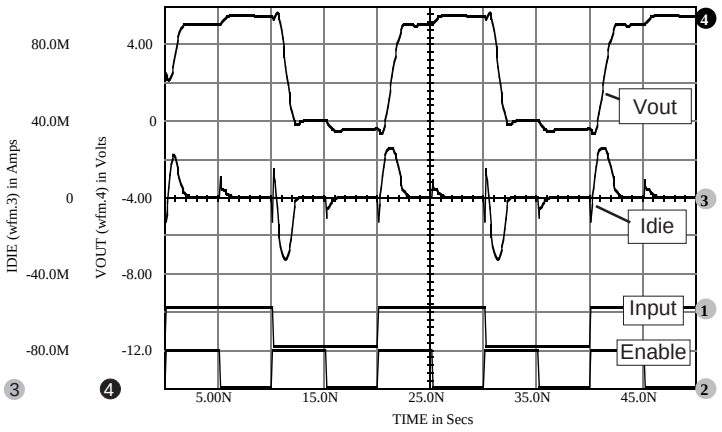


Figure 7, The Intusoft IBIS2 buffer exhibits more realistic off chip current flow (Idie), effects from tristate enabling, and runs faster than the IBIS1 model that uses table functions. Simulation speeds are shown on the opposite page.

version uses the minimum output characteristics, maximum rise/fall time, and maximum package parasitics. The models are included on the newsletter floppy disk and will be posted on the Intusoft CompuServe forum (See page 30-11). By using the Intusoft IBIS1 subcircuit, the user can create models from manufacturer supplied IBIS data. Intusoft will be adding more models as new IBIS data from manufacturer's becomes available.

Conclusion/References

Whether studying crosstalk, ground plane coupling, or other EMC/EMI effects in PCBs, ICs, or backplanes, IsSpice will be able to provide guidance. While it is always best to verify assumptions and obtain actual measured data, SPICE simulation can greatly help the designer understand the electrical behavior of interconnects. In the next newsletter, we will show how to use the IBIS models to represent a load, describe a typical application, and present a further comparison of the IBIS models.

[1] "Efficient Transient Simulation of Lossy Interconnect", J. Roychowdury, D. Pederson, 28th ACM/IEEE Design Automation Conference, 1991

[2] "Simulating Crosstalk and Field To wire coupling With A SPICE Simulator", F. Broyde, E. Clavelier, C. Hymowitz, IEEE Circuits and Devices, Sept. 1992

[3] "Modeling Interconnects", L. Meares, Simulating With Spice, Intusoft 1988

[4] "Analyzing Electrical Effects of Packaging connectors, PCBs, MCMs and backplanes on mixed signal IC and system design", P. Wang, D. Divekar, Analog & Mixed-Signal Design conference, Santa Clara, 1991

[5] "Microwave Circuits, Analysis and Computer aided design", V. Fusco, Prentice-Hall, 1987

[6] "Pentium™ Processor Open Design Guide", Intel, March 1993

FILTERMASTER - Active Filter Design

continued from page 30-1

the standard approximations offered in most other design programs. They include: more freedom in the stopband specification (you can enter an arbitrary tolerance scheme with different loss values, set fixed transmission zeros, and select the number of transmission zeros at extreme frequencies), extra component cost savings from using an exact approximation to the required loss curve, and calculation of unsymmetrical bandpass filters.

Elliptic Bandpass Filter Specifications

Lower passband edge frequency	:	9.000 kHz
Upper passband edge frequency	:	11.000 kHz
Lower stopband edge frequency	:	8.000 kHz
Stopband loss	:	50.00 dB
Passband loss	:	<1.00 dB

The first step in designing the elliptic bandpass filter was to choose the filter type and desired approximation. The five specifications were then entered into the program as shown in Figure 8. Note that the 3 edge frequencies enable FILTERMASTER to calculate the fourth since a symmetrical filter is assumed. At this point, FILTERMASTER allowed us to study the design trade-offs between the filter characteristics (variation in stopband loss vs. passband loss vs. filter degree). Once finalized, FILTERMASTER provided a finished circuit that met all the design criteria. For the values we used, FILTERMASTER proposed an 8th order filter.

FILTERMASTER creates filters in the form of a cascade of first and second order partial filters. The first stage in the elliptic filter is shown in Figure 9. In the dimensioning and arrangement of the partial filters, FILTERMASTER automatically takes into account the optimal modulation and the best possible signal/noise ratio. When scaling the partial filter, the program also takes into account the signal form at the filter's input and the desired

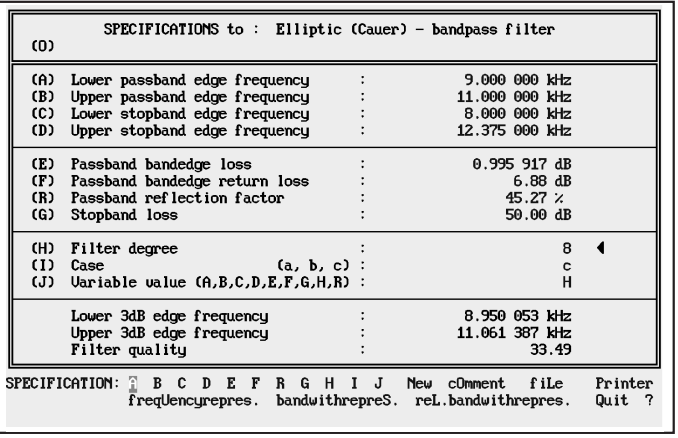


Figure 8, The specifications for an elliptic bandpass filter. FILTERMASTER allows you to perform design trade-offs between various characteristics.

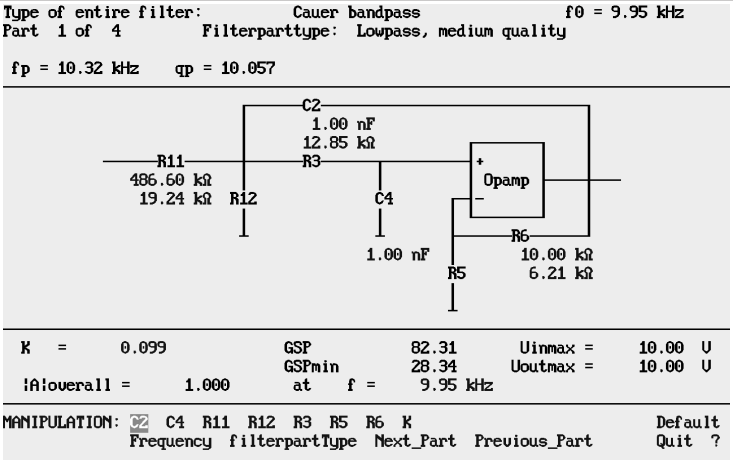


Figure 9, 1st partial filter (out of 4 sections) for the elliptic bandpass shows the part values, gain of the partial filter (K), and gain sensitivity product (GSP, dependence of the transfer function on the open loop op-amp gain).

maximum output voltage. By providing a front-end input amplifier the filter is automatically adjusted to the voltage level of the input signal. This alleviates any possible over-modulation.

FILTERMASTER ACTIVE includes a special dynamic optimization feature that allows filters to be scaled for different input, output, and op-amp voltage levels (Figure 10 bottom). The user can change the maximum input voltage, highest value of the desired output voltage, and the modulation threshold of the op-amp, independently, after the specifications are entered. FILTERMASTER ACTIVE will then automatically recalculate the RC values. This is a unique feature not incorporated in most other

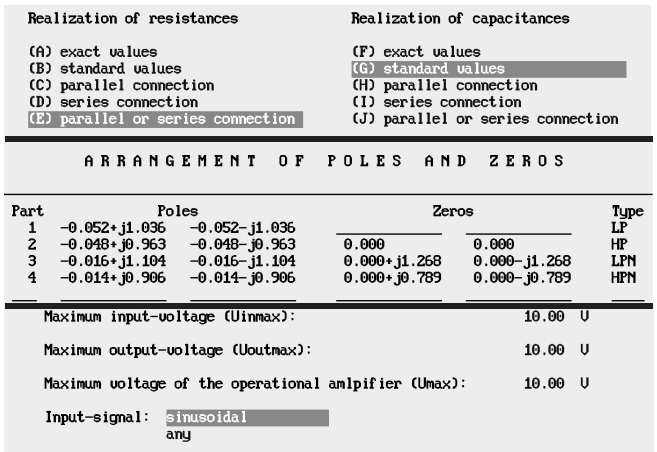


Figure 10, FILTERMASTER ACTIVE gives the user control over the component realization and pole/zero placement. Partial filters can be scaled for different voltage levels.

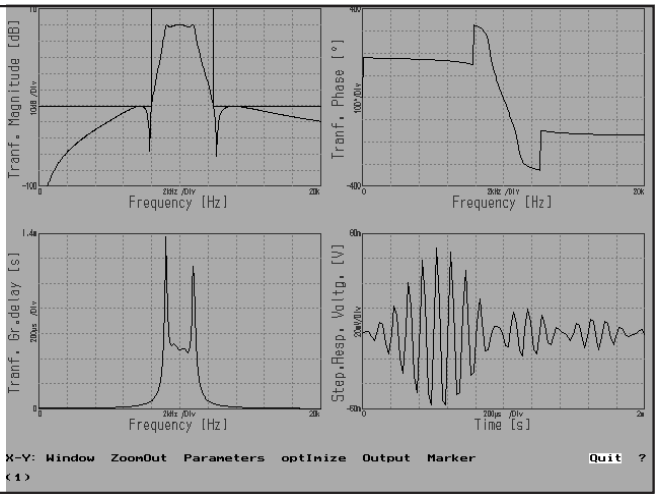


Figure 11, The elliptic bandpass filter's amplitude, phase, group delay and step responses.

active filter design packages and provides a powerful method for component optimization. The program supports the modification of component values, changing of the partial filter amplification, regrouping of the partial filters, rearranging of the poles & zeroes, and substitution of low, medium, and high quality partial filter structures. FILTERMASTER ensures that after each modification step that the specifications are maintained by automatically recalculating the values of all the linked parameters. Component values are either shown as precise values or the best possible match made from a list of standard values. Series or parallel connection of standard values can be chosen (Figure 10). In this design, we have manually set all of the capacitors to the same value, 1nF, in order to reduce costs.

Figure 11 shows the magnitude, phase, group delay, and step response for the 8th order bandpass. The combination of synthesis and analysis in one program allows various filter topologies and characteristics to be easily compared for the optimal results.

Although FILTERMASTER ACTIVE is a stand-alone program, it is smoothly integrated with Intusoft's SPICE based simulation tools. The filter circuit can be transferred directly into the SPICENET schematic entry program as a SPICE subcircuit or saved in a ready-to-simulate stand-alone format. In the next newsletter, we will run a Monte Carlo analysis and test the filter performance as the component tolerances are varied.

FILTERMASTER ACTIVE runs on the PC, requires 640 KB RAM, and DOS 3.0 or higher. Laser and dot matrix printers and HPGL compatible plotters are supported. FILTERMASTER ACTIVE is available now.

FREE IsSpice3 Update On CompuServe

Intusoft's technical support BBS on the CompuServe® Information Service has moved into full swing this month. Posted on the CompuServe CADD/CAM/CAE forum at this time are SPICE models for Fuses, IGBTs, Switched Capacitor Filters, and Dual-Gate Mosfets. Other files include SpiceMod and FilterMaster Passive demos, and a technical article on ***"Solving SPICE Convergence Problems"***. Also posted is a free software update for the IsSpice3 program (from version 3e.2 to 3e.3). You must have the original IsSpice3 program to use the downloaded update. Keep checking the forum as new items will be posted periodically. New items to be posted this month include: Technical articles on RF and power supply simulation, and a variety of new SPICE models. To connect with Intusoft you can navigate through CompuServe's computing support menus to reach the CADD/CAM/CAE Vendor forum or type "Go CADDVEN" at any ! point prompt. Then select the "All CADD/CAM/CAE" section.

You may send and receive mail and files via the CADD forum. Mail messages should be left on the Message section while files can be posted in the Library section. You can also send e-mail directly to Intusoft at our CompuServe address: intusoft@compuserve.com. Internet users can also send e-mail messages to Intusoft using the address format: info@intusoft.com.

New Models Simulate Vacuum Pump Systems

Technology Sources, the Intusoft distributor in the U.K., has developed SPICE models for vacuum pump systems including ion/turbo/rotary pumps, pipes, values, and more. For more information, see http://www.softsim.com.

June ECN Article On Simulating Connectors

There will be an article in the EDA supplement of the June ECN magazine entitled "Simulation Breaks Into New Fields". The article discusses how Ansoft's Maxwell® Spicelink™ software and ICAPS can be used to simulate connectors. Look for it!

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Modeling Corner

The Intusoft

In the past few years hardware manufacturers have begun to produce SPICE models for their components. This positive response, mostly limited to op-amp devices, has been mainly due to customer pressure. In this issue of The Intusoft Modeling Corner we will bring you up to date on one company that has forged a new modeling path. Philips Semiconductors is one of the first companies to come out with models for discrete devices. At this time, models for JFETs and RF bipolar transistors are available. Figure 12 shows two of the JFET models. The RF frequency BJT models come in two parts; the SPICE Gummel-Poon .MODEL statement, and the package parasitics. Figure 12 shows how the two are combined to make a valid model for a specific part. SPICE netlists for over 100 JFET and 75 BJT devices are stored in the newsletter floppy for subscribers. BJTs and JFETs in the 2N, BC, BF, BS, J, MPSH, PMB, and PZF series are included.

On another front, Philips has produced models for their ALS, ABT (BiCMOS), Multibyte™, FAST, Futurebus+, and LVT (a 3.3V BiCMOS logic family) families. The models are available directly from Intusoft. These models are different from the Intel IBIS models. Philips' models are based more on the exact transistor topology. Therefore, the subcircuit topology is not process independent, but the models are extremely accurate and the Philips offering is very comprehensive.

```
.MODEL  JN4091  NJF VTO = -8.0337E+000 BETA = 1.56450E-003 LAMBDA = 1.00000E-002
+ RD = 8.25115E-001 RS = 8.25115E-001 IS = 6.54620E-016 CGS  = 8.75000E-012
+ CGD  = 1.37500E-011 PB = 7.72344E-001 FC = 5.00000E-001
********
.MODEL  J174   PJF VTO = -7.1507E+000 BETA = 1.24461E-003 LAMBDA = 2.01968E-002
+ RD = 3.95403E+000 RS = 3.95403E+000 IS = 9.72750E-016 CGS  = 1.58000E-011
+ CGD  = 1.88000E-011 PB = 3.72072E-001 FC = 5.00000E-001
********

.SUBCKT BFR92A  1  2  3
CBE 4 5 71FF
CCB 4 6 71FF
CCE 5 6 2FF
L1 2 4 .35NH
L2 6 1 .17NH
L3 5 3 .35NH
LB 4 7 .4NH
LE 8 5 .83NH
Q1 6 7 8 BFR90A
.MODEL  BFR90A   NPN IS = 4.11877E-016 BF = 1.02639E+2 NF = 9.97275E-001 VAF = 6.26719E+1
+ IKF = 3.20054 ISE = 4.01062E-015 NE = 1.57708 BR = 1.81086E+001 NR = 9.96202E-001
+ VAR = 3.36915 IKR = 1.28155 ISC = 2.79905E-016 NC = 1.07543 RB = 1.0E+001 IRB = 1.0E-006
+ RBM = 1.0E+001 RE = 1.16450 RC = 2.320 EG = 1.110 XTI = 3.0 CJE = 8.90512E-013
+ VJE = 6.0E-001 MJE = 2.58570E-001 TF = 1.54973E-011 XTF = 3.91402E+001 VTF = 2.15279
+ ITF = 2.13776E-001 CJC = 5.46563E-013 VJC = 3.80824E-001 MJC = 2.02935E-001
+ XCJC = 1.50E-001 TR = 5.61796E-009 VJS = 7.50E-001 FC = 8.50E-001
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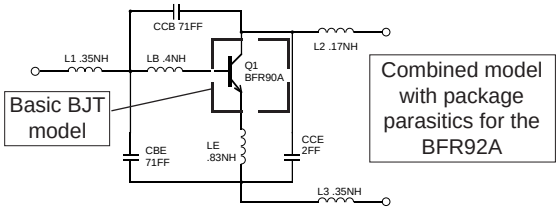

Figure 12, Shown at the top are models for 2N4091 (N Channel) and J174 (P Channel) JFETs. The BFR92A RF BJT subcircuit is shown below.

The models are mainly to be used as drivers and loads in the process of simulating PCB interconnect problems. Models for each family consist of a series of different input and output stages. The input stages can be used as loads, while the output stages are used as drivers. Complete models for a particular device can be created by concatenating an input stage with an output stage. Intermediate inverting sections and external package parasitics can also be added to the input/output combination. Figure 13 shows an example of the input and output stages for the ABT125. Also shown is a typical example using the FAST logic. Several loads are connected to a backplane and a signal is driven from one of the output stages.

SPICE models for each of the families listed previously, as well as “canned” models for specific devices, are included on the newsletter floppy disk along with documentation on which input/output subcircuits go with each specific component.

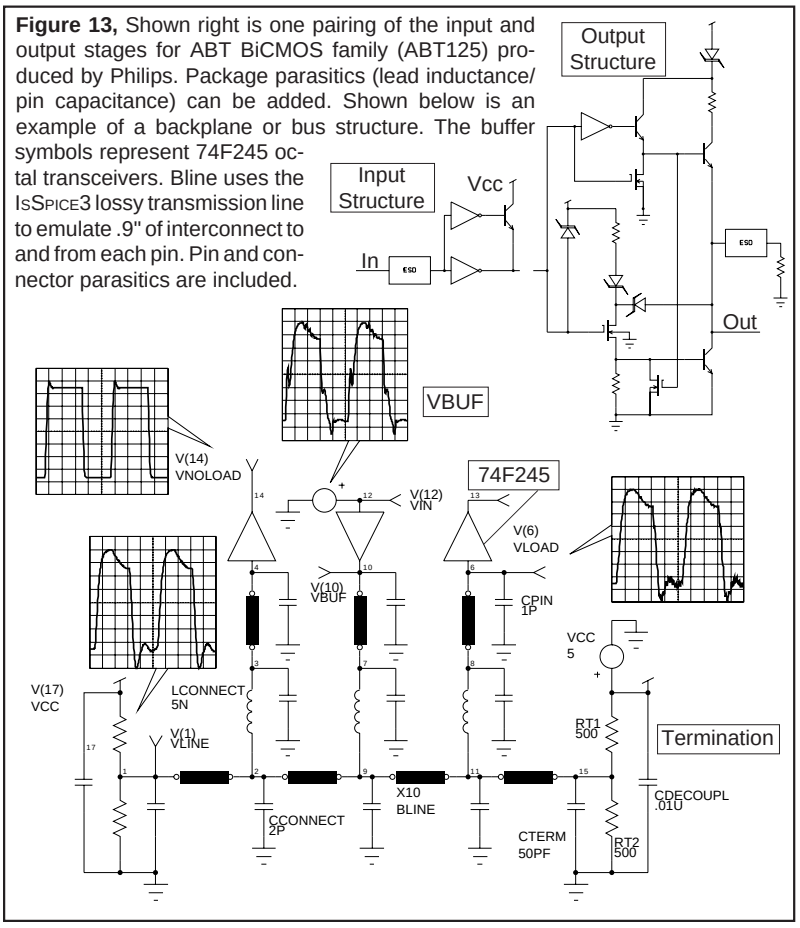

Figure 13, Shown right is one pairing of the input and output stages for ABT BiCMOS family (ABT125) produced by Philips. Package parasitics (lead inductance/ pin capacitance) can be added. Shown below is an example of a backplane or bus structure. The buffer symbols represent 74F245 octal transceivers. Bline uses the IsSpice3 lossy transmission line to emulate .9" of interconnect to and from each pin. Pin and connector parasitics are included.

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