Intusoft Newsletter

Personal Computer Circuit Design Tools

February 1992 Issue

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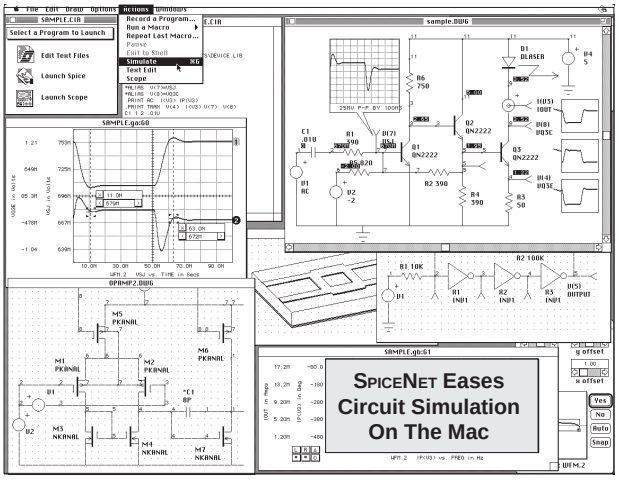
NEW SPICENET SCHEMATIC ENTRY RELEASED

Intusoft has introduced the first schematic entry program for the Macintosh especially designed for analog and mixed signal simulation. With SPICENET v3.0M, Macintosh users finally have a completely integrated front to back simulation system. The NEW SPICENET schematic entry program completes Intusoft's current line of circuit simulation products including SPICE model libraries, circuit simulation and waveform processing. SPICENET provides netlists for all popular SPICE simulators including Intusoft's own ISSPICE.

In This Issue

SPICENET 3.0M, and its counterpart for PC platforms, version 3.0, is unlike any other schematic entry package. It is fine-tuned for entering analog circuit designs and generating netlists for the SPICE analog circuit simulator. All the facets of SPICE netlist generation are supported including connectivity, control statements, SPICE options, model library access, syntax extensions, and subcircuits. Node numbers and reference designations are automatically generated. No editing of the netlist is required at all. Symbol support for thousands of devices is also included, making symbol creation unnecessary. However, a flexible symbol creation option is always on-line in SPICENET allowing the designer to make symbols “on the fly”.



(Continued on Page 24-10)

Simulating Circuits With SCRs

When modeling devices for simulation, the best model is one that accurately emulates the real part, simulates efficiently, converges well, and is easy to create. A new SCR model, implemented in the forth coming version of the SpiceMod, SPICE modeling spreadsheet program, is just such a model. This article explains the model, which is based on the two transistor [1,2] and four transistor Intusoft model [3], and provides an example of its use.

The Basic SCR Model

Figure 1 shows the design of a typical planar "shorted emitter" SCR and the classical two transistor combination used to model the positive feedback effects of the four semiconductor layers. The NPN transistor models the three layers at the cathode end and the PNP transistor models the three layers at the anode end. The two center layers are common to both transistors.

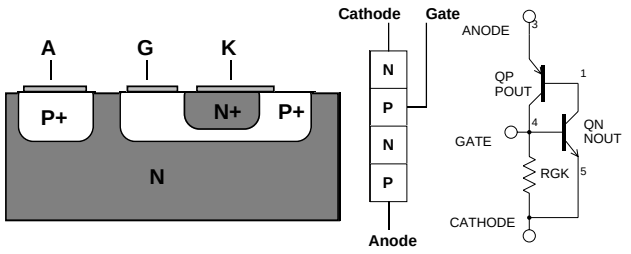


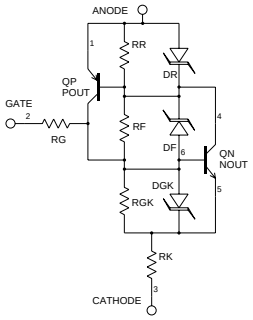
Figure 1, Cross section of a planar shorted emitter SCR and its basic equivalent representation using NPN and PNP transistors.

The cathode (emitter) metallization overlaps the gate (base) of the NPN transistor, forming a leakage path to carry leakage currents around the gate until the gate is triggered from an external source. This is shown as RGK in the model.

The base of each transistor is connected to the opposite collector forming positive feedback as soon as both base-emitter junctions become forward biased. Although this model has the triggering function of an SCR, it must be enhanced to emulate other parameters such as off state leakage, break-over voltage and current, reverse breakdown characteristics and dv/dt turn-on.

SpiceMod Improves The SCR Model

Figure 2 shows the additions to the basic model. Table 1 lists a sample .SUBCKT netlist from the PreSpice libraries. For *Intusoft Newsletter* subscribers, several additional new SCR models have been included on the enclosed floppy disk. The availability of the new SpiceMod program, containing new SCR, IGBT, and Zener models will be announced in the next newsletter.




```
SPICEMOD 2.0 ==================== SCR (X) ======================== 02-05-1992

                    .SUBCKT Name (S2M4171) = S2M4171        Affects:
Peak Repetitive Forward Blocking V., VDRM =   300.000 V    BV(ZF), RF
Peak Repetitive Reverse Blocking V., VRRM =   300.000 V    BV(ZR), RR
    Gate to Cathode Reverse Voltage, VRGM =     5.000 V    BV(ZGK)
                RMS Forward Current, IT(rms) =     8.000 A   (Scales all Values)
                        Peak Gate Current, IGM =     2.000 A    RG
                        Peak Gate Voltage, VGM =    10.000 V    RG
    Peak Forward Blocking Current, IDRM =     1.000 mA   IBV(ZF), RF
    Peak Reverse Blocking Current, IRRM =     1.000 mA   IBV(ZR), RR
                Gate Trigger Current,  IGT =    10.000 mA   RGK
                Gate Trigger Voltage,  VGT =     0.750 V    RGK
                 Forward (on) Voltage, VTM =     1.400 V    RK, RC
              at Current (near 2*IT), ITM =    16.000 A    RK, RC
                        Holding Current,  IH =    10.000 mA   RGK
            Turn-On Time (td + tr), t(on) =     1.000 us   TF
                        Turn-Off Time, t(off) =    15.002 us   TR
  Forward Voltage Application Rate, dv/dt =    50.000 V/us CJC, CJE
                                at VD =   300.000 V    CJC, CJE


                    (TO SEE SPICE PARAMETERS, PRESS 'F2')

  SELECT WITH ARROWS, TYPE NEW DATA   F1=HELP   F3=RESET ALL     Esc WHEN DONE
```

Figure 2, SPICEMOD takes the data sheet parameters shown above and generates an ISSPICE .SUBCKT model (schematic on left) for the SCR. Parameters not available will be estimated by SPICEMOD based on the data that is entered insuring a realistic model.

Forward Break-over/Reverse Characteristics

The following parameters are used to calculate various forward and reverse characteristics. Only parameters that are generally available in data sheets are used because this is normally the only data that engineers have access to.

Parameters For Forward Break-Over and Reverse Characteristics

VDRM = Max. Forward Voltage	VRRM = Max. Reverse Voltage
IDRM = Leakage Current @ VDRM	IRRM = Leakage Current at VRRM
VRGM = Max. Reverse Gate Voltage	IT = RMS Forward Current
VGT = Gate Trigger Voltage	IGT = Gate Trigger Current
IH = Holding Current	

QN, the NPN transistor, has a forward beta of 100 and contains the gate at its base. QP, the PNP transistor, has a forward beta of one to emulate the (lower gain) high voltage junction near the anode. The resistor RF emulates the forward leakage current when the SCR is "off" (QN is off, but QP is on). Zener diode DF sets the breakdown voltage in the forward direction. Internal series resistance, RS, is added to this diode to produce a rounded peak.

$$RF = (BFp + 1) * VDRM / IDRM \quad (1)$$

where BFp = BF of QP (set at 1)

for DF:

$$BV = VDRM \quad (2)$$

$$IBV = IDRM / 10 \quad (3)$$

$$RS = RF / 10 \quad (4)$$

Resistor RR emulates the leakage when the SCR is reverse biased. The base-emitter junction of QP sees most of the voltage in this mode. The zener diode, DR, sets the reverse breakdown point. Diode DGK serves a similar function for QN, but its breakdown voltage is set between five to seven volts (VGR).

Forward /Reverse Characteristics *con't*

RR = VRRM / IRRM (5)

for DR:

IS = .001 ∗ ISp (6)
BV = VRRM (7)
IBV = IRRM / 10 (8)

for DGK:

IS = .001 ∗ ISn (9)
BV = VRGM (10)
IBV = IDRM / 10 (11)

Because these diodes shunt the base-emitter junctions, their IS (leakage current) is made 1000 times smaller than the IS of the transistors to minimize their effect on these junctions. It is also important not to use any base or emitter resistance (RB, RE) in these transistors as they would cause voltage drops that would forward bias the diodes, robbing current from the transistors.

Gate Characteristics

Parameters Used For Gate Characteristics

IGM = Peak Gate Current	VGM = Peak Gate Voltage
VTM = Forward (on) Voltage	ITM = Forward (on) Current

It is necessary to add a cathode resistance to emulate the increase in gate voltage with cathode current. RK serves this function. The rest of the “on” voltage is simulated with model parameter RC in QN, eliminating the need for an additional external part. A gate resistor, RG, has been added to properly simulate the resistance found when over-driving the gate.

R(sat) = (VTM - VD) / ITM (12)
RK = .2 ∗ R(sat) (13)
RC = .8 ∗ R(sat) (14)
RG = ((VGM - VD) / IGM) - RK (15)
where VD = B-E diode drop (approx. VGT)

Because this model has separate resistors shunting each junction, convergence is improved over other models.

Dynamic Characteristics

Switching time limits are modeled using NPN/PNP charge storage model parameters. Note that TF is the forward transit time, not the fall time, and TR is the reverse transit time, not the rise time.

TF = .179 ∗ t(on) (16)
TR = 1.7 ∗ t(off) (17)

Parameters Used For Dynamic Characteristics

t(on), td+tr = turn-on Time t(off), tq = turn-off Time
dv/dt = Forward Voltage Application Rate

The dv/dt limit is reached in an SCR when a change in the anode voltage flowing through the output capacitance (COE) causes sufficient current to flow in the gate circuit to turn the SCR on. The effective collector capacitance (CJC) can be calculated using the dv/dt specifications:

$$COE = IH / dv/dt \quad (18)$$

$$CJC = COE \text{ (adjusted for test voltages)} \quad (19)$$

$$= COE * (1+VD/VJE)^{MJE} \quad (20)$$

where VJE=.75 and MJE=.33 (IsSpice default). The input capacitance, which is seldom given in data books, is estimated at five times the collector capacitance:

$$CJE = 5 * CJC \quad (21)$$

```
.SUBCKT C180    1 2 3
*   TERMINALS:  A G K
* Powerex 100 Volt  150 Amp  SCR
QP  6 4 1  POUT OFF
QN  4 6 3  NOUT OFF
RF  6 4    10K
RR  1 4    6.66K
RG  6 3    10
RGS 2 6    4.66M
DF  6 4    ZF
DR  1 4    ZR
DG  6 3    ZG
.MODEL ZF   D (IS=94F IBV=2M BV=100 RS=1.5K)
.MODEL ZR   D (IS=94F IBV=2M BV=133)
.MODEL ZG   D (IS=94F IBV=2M BV=5)
.MODEL POUT PNP (IS=94P BF=1 CJE=37.8N TF=337N TR=170U)
.MODEL NOUT NPN (IS=94P BF=100 RE=233U RC=233U
+ CJE=37.8N CJC=7.56N TF=337N TR=170U)
.ENDS
```

Table 1, IsSpice subcircuit listing for the Powerex C180 phase control SCR with VDRM=100V and IT(avg)=150A.

Simulating A Resonant Regulator

Using a model for an SCR, (Philips BTW38) a simple resonant buck regulator (Figure 3) was constructed. The L1/C2 combination has a resonant frequency of 4kHz. The SCR is controlled by the pulsed current source, I2. Of note is the fact that the damping network across diode D1 is needed to reduce ringing at the cathode which might turn the SCR on. Without the R/C network, the SPICE simulation may abort unless the .OPTIONS parameters RELTOL is relaxed to .01. The constant current source I1, models a constant load. In order to achieve a steady state response at the beginning of the simulation, its value must be adjusted to the average value of the current flow in the inductor.

Conclusions

A SPICE SCR subcircuit has been developed that relates well to data book parameters. It emulates both the forward and reverse characteristics while avoiding convergence problems. However, the breakdown behavior, emulated in this and other models, may cause convergence problems due to various cascading

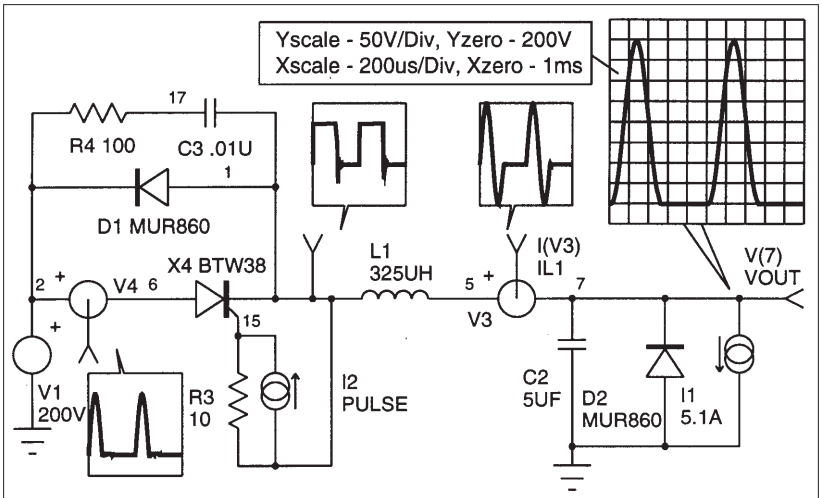


Figure 3, Using the new SCR model, a resonant buck regulator circuit can be simulated.

nonlinearities. Therefore, aborted simulation results should be checked to see if the device ratings were exceeded, especially near the end of the simulation. Sensitive gate SCR devices can be modeled because the internal RGK will generally have a large value, thus allowing the addition of an external resistor. GTOs, which are similar to SCRs except for a smaller gate resistor, can also be modeled by putting in the proper Peak gate current and voltage.

References and Biography

[1] "A Practical SCR Model for Computer Aided Analysis of AC Resonant Charging Circuits", R.L. Avant, F.C. Lee, and D.Y. Chen, IEEE, July, 1981.

[2] "A SPICE Model for the SCR", Waiman, F. Ki, Master Thesis, Department of E & CS, UC Berkeley, Dec., 1979.

[3] "PreSpice User's Guide", Intusoft, 1991.

[4] "Semiconductor Device Modelling with SPICE", Paolo Antognetti and Giuseppe Massobrio, McGraw-Hill, 1988.

[5] "Bipolar Power Transistor and Thyristor Data", Motorola Inc., DL111, REV3, 1984.

A great deal of thanks goes to the author of this article and developer of SpiceMod, the SPICE modeling Spreadsheet. A. F. "Slim" Petrie. Mr. Petrie is retired from Motorola Inc., where he was a Principal Staff Engineer and Dan Noble Fellow. He develops both hardware and software and holds 24 U.S. Patents. His "Circuit Analysis" program was sold through Apple computer in the early 1980s. With a keen appreciation for the problems of the working engineer, he continues to develop tools to make that job easier. He can be reached at 7 W. Lillian Ave., Arlington Heights, IL 60004, where he welcomes your comments.

New Models Simulate RF Circuits

Part II

In part I of this application note we set out to simulate a 500MegHz RF oscillator circuit. The schematic is repeated here for clarity (Note that the inductor LCX was previously shown at the wrong value; the correct value is 5nH.) In part II, the results of the simulation with and without critical circuit parasitics will be shown.

In the first case, the circuit was simulated with two inductor chokes, LSP and LEC, and a standard Gummel-Poon representation for the transistor, 2N5109. In the second case, the chokes were each replaced with the new RF bead model and the transistor with a subcircuit representation containing package parasitics. (See Nov. 1991 issue) Parasitics for the passive elements were maintained for both cases.

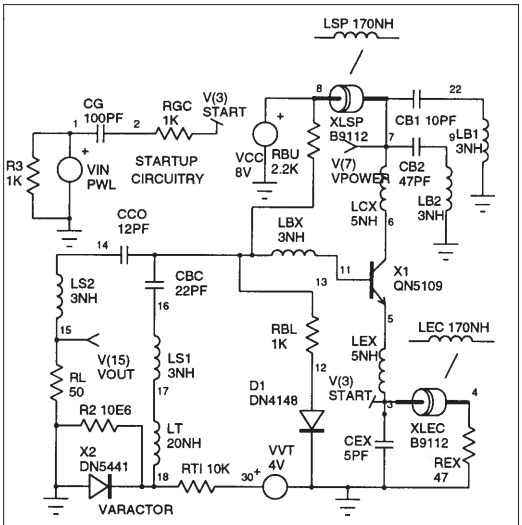


Figure 4, A 500 MHz oscillator. Use of inductors or RF beads reveals vastly different responses.

In order to isolate VCC and not contaminate the power supply with the 500 MHz oscillating waveform, adequate bypassing is required. A voltage generator represents a perfect bypass because it is 0 ohms at all frequencies. This is quite different from the real world.

As shown in Figure 5, use of an inductor causes a droop in the VCC voltage. The reason for the droop is that the 170nH represents a large impedance. As the oscillator starts, the transistor wants more current. Because of the large inductance it can't draw adequate current so it starts to discharge the bypass capacitors. This appears as a drooping in the VCC power (lower graph). The bead, on the other hand, has a very low DC impedance and a high AC impedance. By choosing the proper bead, a frequency response can be selected that will block all the AC around the oscillation frequency. With the bead (upper graph), the VCC line doesn't droop and shows that the size of the ripple stays the same revealing the imperfections in the bypassing. Also note that the oscillation starts slower and does not have quite as much power out with the bead inserted (to be expected) as it does when the inductors are used.

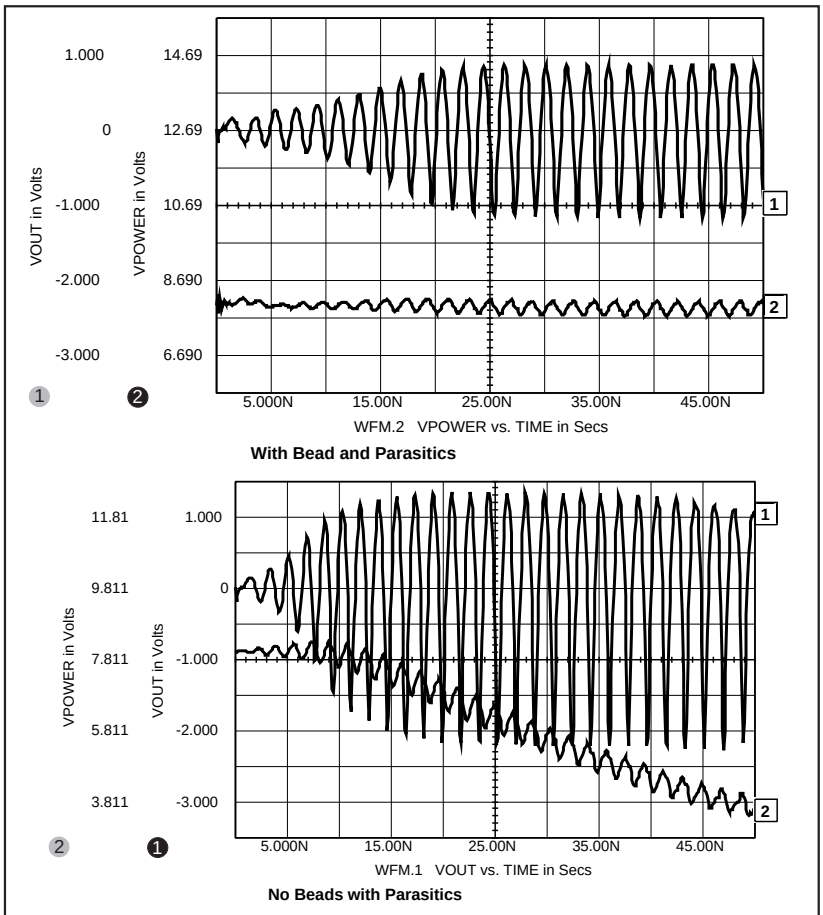


Figure 5, Comparison of the start-up and power supply waveforms with (Top) and without (Bottom) the new RF bead model.

The oscillator with no BJT parasitics or beads still oscillates because it was made to be tolerant of package parasitics, but the results predicted were inaccurate in several important areas. As shown in Figure 6, the FFT and transient response of the circuit with beads and new RF BJT subcircuit model reveals that the frequency of oscillation is lower and the distortion higher.

Conclusions

From the simulations performed, it is clear that modeling the proper circuit parasitics is of vital importance, especially at RF frequencies. It is recommended that initial simulations run for many cycles in order to verify that stable oscillation is actually taking place. As for performing an FFT, the IsSpice .TRAN tstart parameter can be used to delay the start of data taking until steady state oscillation has been reached.

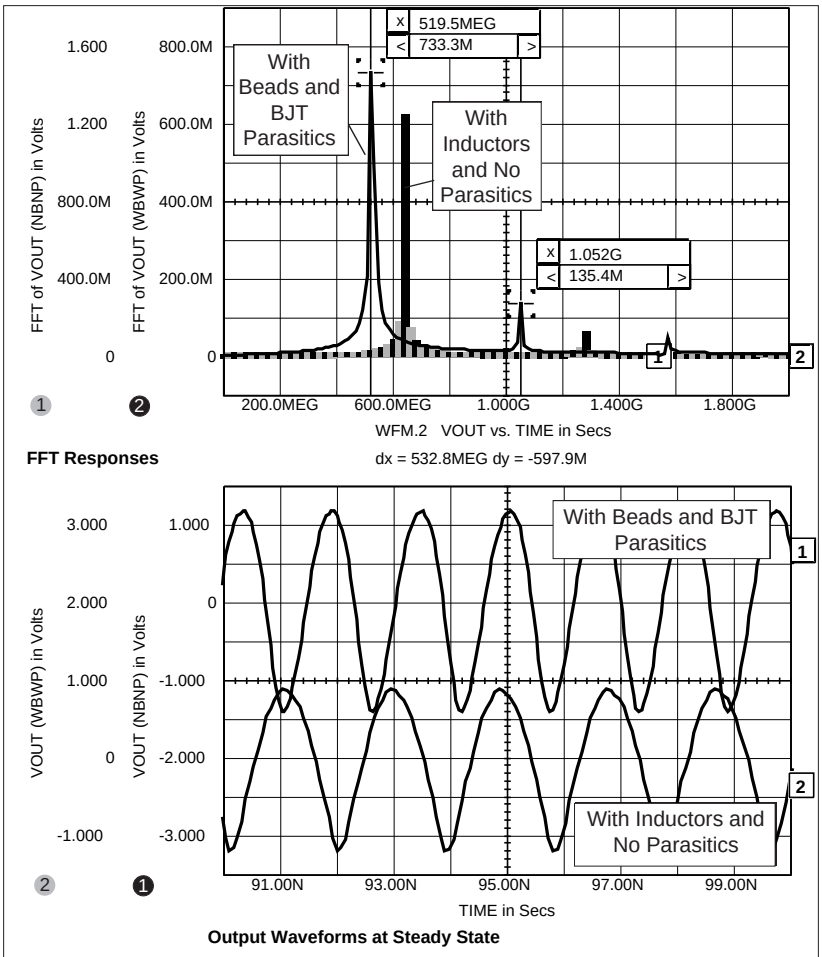


Figure 6, Comparison of the frequency spectrum and time waveforms using the new BJT and bead models vs. the Gummel-Poon model and inductor chokes. Notice the more accurate prediction of distortion and oscillation frequency with the new models.

With the new bead and BJT models in the RF library, IsSpice is able to show the peak component stresses when power is applied, the transient start-up performance, and the variations in the power supply. In contrast to the linear analysis programs commonly used by RF designers, IsSpice simulations can reveal many important circuit properties such as efficiency, power dissipation, and harmonic distortion. Characteristics that would be either difficult or impossible to measure. In a future application note, we will explore an even more challenging circuit, that of a class C RF power amplifier.

Note: Thanks to Bill Sands of Analog & RF Models, specialists in the creation of RF device models for his suggestions and comments.

New Features Make SpiceNet Tops

cont'd from page 24-1

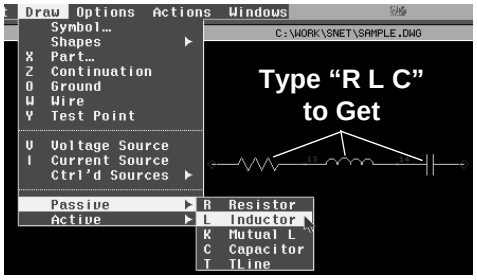
The new SpiceNet 3.0 version has many new features that make it extremely versatile and fully integrated with your SPICE program. For instance:

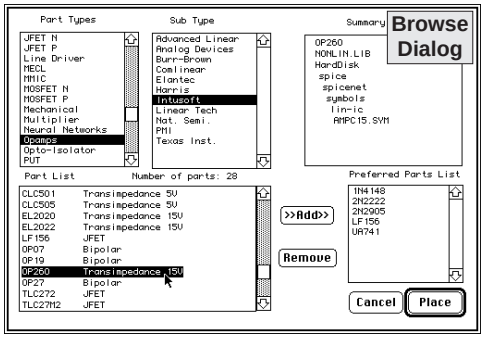
Macintosh and PC Support

SpiceNet 3.0 is now available for the Macintosh and for the PC (All Platforms). The programs are virtually identical in their look and operation. The schematics that are produced are transferable between the two systems.

SPICE Compatibility

The netlist generated by SpiceNet is compatible with all PC and Macintosh SPICE versions. There's even the flexibility to assign your own key letters to any SPICE element, as well as the ability to enter vendor specific SPICE syntax extensions. The component and symbol databases can be easily updated and augmented by the user.





Fast Part Placement

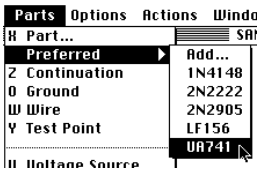
All SPICE primitive symbols (resistors, BJT's, etc.) can be placed with 1 keystroke. This is a distinct contrast to other schematic programs which require a number of keystrokes or menu selections. There is also a browsing capability (shown left) that can access over 1800 parts in Intusoft's user editable SPICE model database. This includes a wide variety of IC SPICE models supplied by independent hardware vendors like TI, National, and Analog Devices. The Browse window contains a short description of the device and allows parts to be placed by their part number.

Multiple Schematics and Pages

Several schematics can be displayed and edited at the same time in different windows using Intusoft's graphical user interface. The added ability to cut and paste between

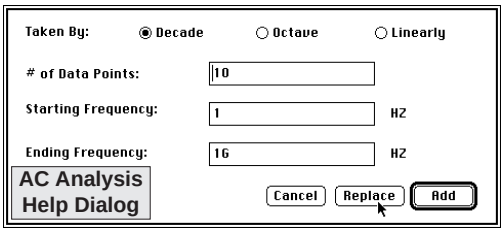
different pages and different schematics allows an engineer to easily build circuits using pieces from old designs.

Preferred Parts list



Frequently used parts can be placed on a preferred parts list submenu. Together with the Browse feature and the single letter symbol placement, SPICENET is the fastest and easiest program available for drawing analog/mixed signal schematics.

Simplified Controls Statement Support



SPICENET has a dedicated text window allowing advanced users to enter SPICE control statements quickly. For novice or infrequent users, special help dialogs that prompt the user in plain English for the proper variables are available. The help dialogs then construct the proper SPICE syntax for the user. The dialogs can also “load in” a previously entered SPICE statement, allowing quick update and easier learning of SPICE syntax.

One Integrated Simulation System

SPICENET is completely integrated with all of Intusoft's simulation tools through the ACTIONS menu. This feature allows users to select any simulation task with a simple menu selection.

On Line Help & Improved Printer Support

The printing and plotting capabilities of SPICENET (PC) have been greatly enhanced to include support for Postscript, HPGL/2, TIFF, and EPS formats, in addition to the standard HP Laser (PCL) and Epson/IBM compatible printers and HP/Houston Instruments plotters. For Macintosh users, any device in the Chooser can be selected.

The Intusoft Modeling Corner

This is a new column for the *Intusoft Newsletter*. In the Modeling Corner you will find brief explanations and listings of recently developed models from the Intusoft Tech Support Department.

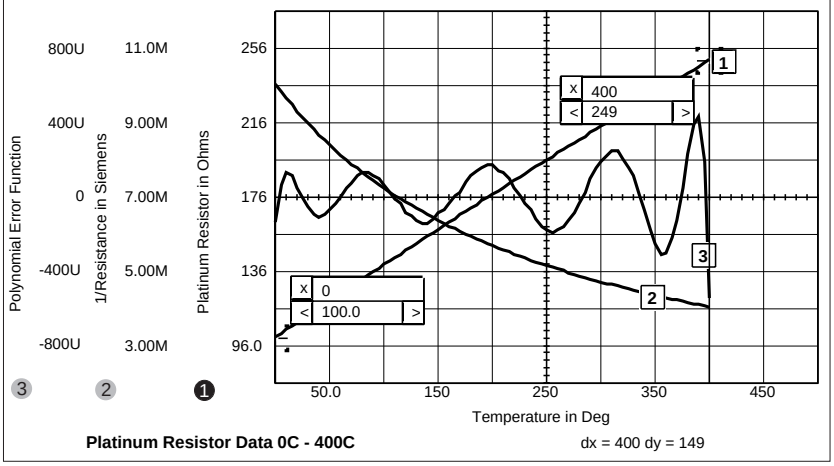
Last month, Intusoft was asked to simulate a circuit for an EDN magazine article (due out in May) which needed a model for a platinum resistor thermal sensor. After contacting the vendor (Thanks to Stacy Longton; Marketing Engineer at Rosemount Inc.), the temperature vs. resistance data was entered into a simple SPICE-like text file. IntuScope, which can read user generated data files, displayed the data (Waveform 1), calculated the conductance (Waveform 2) and found a 9th order polynomial. The resulting coefficients were used to construct an Analog Behavioral model consisting of a voltage controlled voltage source and the Intusoft switch model. The VCVS element takes in a voltage equal to the temperature. The output of E1 then controls the switch (G1), which acts as a voltage controlled resistor (R=1/V). This allows IsSpice to sweep the temperature of the sensor by sweeping Vin. Higher order polynomials can be calculated to further reduce the error (Waveform 3).

```
.SUBCKT PLATRES 1 2 4
Connections   In+ In- Temperature(Vin)
E1 3 0 4 0  9.9999852M,  -39.578240U,  162.20918N,  -651.71860P,
+ 2.4374024P,  -7.7566684F,  1.8935112E-17,  -3.1854041E-20,
+ 3.2138513E-23,  -1.4483587E-26,
G1 1 2 POLY(2) 1 2 3 0 0 0 0 0 1
RE1 3 0 1E12
RIN 4 0 1E12
RG1 1 2 1E12
.ENDS
```

Platinum Resistor Thermal Sensor Subcircuit

Good For 0C to 400C

Figure 7, Schematic and graph of the platinum resistor response. IntuScope calculates the polynomial coefficients and displays the resulting error waveform.



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