intusoft (213) 833-0710 *Personal Computer Circuit Design Tools*

N E W S L E T T E R

NEW VERSION OF INTU_SCOPE DEBUTS AT WESCON: Featured in this newsletter is Intu_Scope version 2.0, an update of version 1.2 featuring EGA and Hercules monochrome compatibility, statistical grids and over 40 new functions. The code has grown from just under 100K bytes to nearly 170K bytes. Added functions include:

Inverse, complex FFT
Filter windows
Smoothing
Polynomial regression
Piece wise linear file generation
6 Trigonometric vector operations
5 Transcendental vector operations
Polar—Rectangular conversion
Rotation
Conditional branching
Waveform shift with 0 fill
Units/Name entry

A macro keystroke capability has been added so that you can build up to 10 macros using alt-function keys, each with up to 500 keystrokes, to execute measurements such as rise time and propagation delay.

The pixel limit has been doubled and the waveform limit of 500 data points has been removed by providing a delay in waveform acquisition.

IBM and Okidata printers are now handled directly without using the PRINTER.EXE program.

The statistical grids are HISTOGRAM and PROBABILITY. The Histogram Grid will automatically calculate a ½ sigma cell size and output mean and standard deviation.

The Probability Grid warps the X axis, on which percent probability is shown, such that a Gaussian distribution is plotted as a straight line. The data file is automatically sorted. This format is great for "eyeballing" distribution functions, even when the sample size is small. Both grids shown in the figures below illustrate the two formats. The data from the August newsletter is shown using the new grids on an EGA resolution screen.

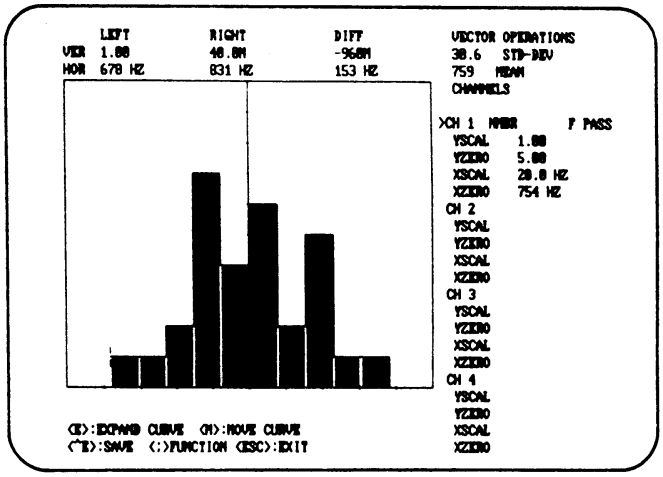

Figure 1, Histogram of elliptic filter pass band variation

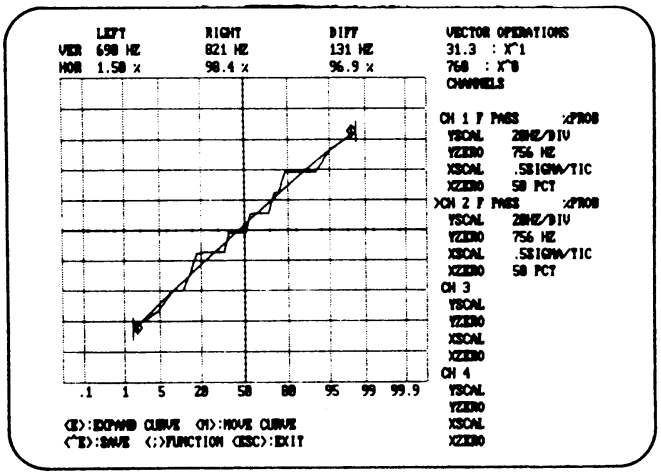

Figure 2, Cumulative probability and least squares polynomial curve showing elliptic filter pass band variation

The "straight" line overlaying the cumulative probability plot was made by asking for a fourth order polynomial regression analysis of the probability data. The first two terms seen in the accumulator and stack correspond to mean and standard deviation, higher order terms are small, as would be expected for a normal (Gaussian) distribution.

Also to be previewed at WESCON is an IS_SPICE schematic entry program. It will produce an IS_SPICE source and plotter driven schematics. Intended to be a low cost alternate method of entering data, the package has eliminated many features needed for production schematics and circuit board layout in order to keep it simple and inexpensive. This program will be available in 1987 as part of an enhanced plotter package.

* * * * * APPLICATION NOTE * * * * *

This application note will cover several topics associated with SPICE modeling, showing how the new version of Intu_Scope can be used to help define model parameters. The bibliography following this note will provide references for those interested in more information. If you have any interesting applications you would like to share, please send them to us for use in a future newsletter.

DIGITAL CIRCUITS: There have been questions regarding the use of IS_SPICE for digital simulations. Digital circuits that use building blocks such as gate arrays or discrete logic families are best analyzed using one of the logic timing and verification programs currently on the market. The effort required to get an equivalent IS_SPICE analysis would not be warranted. If, on the other hand, a custom circuit is being developed or if mixed analog and digital circuits are used, IS_SPICE or mainframe SPICE should be used, perhaps in conjunction with a logic simulation.

When modeling a mixed analog/digital circuit, the behavior of the logic elements may only be needed to control the analog process. While exploring the options for making efficient digital macro models, the idea of using threshold logic was suggested. A threshold gate takes its binary inputs as two valued analog signals. The sum of each signal, multiplied by a weighting constant forms an analog value that is compared to a threshold value. If the sum is greater than a threshold, then an analog voltage is output that represents one logic state, otherwise the analog of the other logic state is output. The table below shows how this works for a three input nand gate.

TABLE 1, Threshold logic description of a 3 input NAND gate.

A	B	C	SUM	<A,B,C>2:3	<A,B,C>3:2	
0	0	0	0	0	1	
						or/nor threshold
0	0	1	1	0	1	
0	1	0	1	0	1	
0	1	1	2	0	1	
1	0	0	1	0	1	
1	0	1	2	0	1	
1	1	0	2	0	1	
						and/nand threshold
1	1	1	3	1	0	

The separating function 2:3 says to output 1 if SUM is between 2 and 3, the 3:2 function outputs the opposite logic state to make a nand gate. Notice that an "or" gate would use the separating function 0:1.

The analog nature of the IS_SPICE simulator makes the threshold approach attractive if it is possible to make a function that separates the sum of inputs into two values of outputs. We tried the polynomial function, using Intu_Scope to find a polynomial using the new regression feature. The resulting function, shown below, was used to test the three input threshold nand gate.

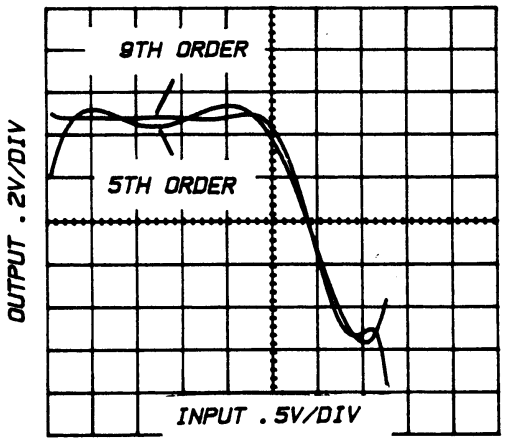

Figure 3, Polynomial function used for a threshold gate
Fifth order and ninth order polynomials shown

Polynomial functions work best, in the sense of best accuracy, for smooth functions that increase from zero toward infinity. Functions that go to zero or a constant at infinity can be modeled over some region, however, the functions will grow toward plus or minus infinity outside that region. While we may not be interested in operation outside of the defined region, the IS_SPICE simulation may move outside the specified region during the analysis, yielding an unstable result.

Notice that our function violated the rule, however, it was defined with a guard band about the expected operating region. The figures shown here are for the ninth order function.

The nand subcircuit includes a capacitor at the output in order to provide a means of initializing the gate and to provide a delay that may be necessary for some logic circuits.

Figure 4 shows the gate performance for a time varying input that exercises all states. The listing shown below generated these data.

TABLE 2, PRE_SPICE listing for a Threshold NAND gate

```
NAND TEST
.OPTIONS ACCT RELTOL = .01
.TRAN 1NS 100NS
.PRINT TRAN  V(1)  V(2)  V(3)  V(4)
VIA 1 0 PULSE 0 1 0 1NS 1NS 9NS 20NS
VIB 2 0 PULSE 0 1 0 1NS 1NS 19NS 40NS
V1C3 0 PULSE 0 1 0 1NS 1NS 39NS 80NS
X1 1 2 3 4 NAND3 {IC = 1.0}
.SUBCKT NAND3 1 2 3 4
E1 5 0 POLY(3) 1 0 2 0 3 0 0 1 1 1
G2 0 4 5 0
+ 1.002290E0,2.624314E - 3, - 1.491959E - 1,8.325288E - 2,
  1.321210E0,
+  - 3.086306E0,2.880211E0, - 1.322610E0,2.952994E - 1,
   - 2.558351E - 2,
R1 1 0 1E12
R2 2 0 1E12
R3 3 0 1E12
R4 4 0 1
R5 5 0 1E12
C1 4 0 .87NF IC = {IC}
.ENDS
.END
```

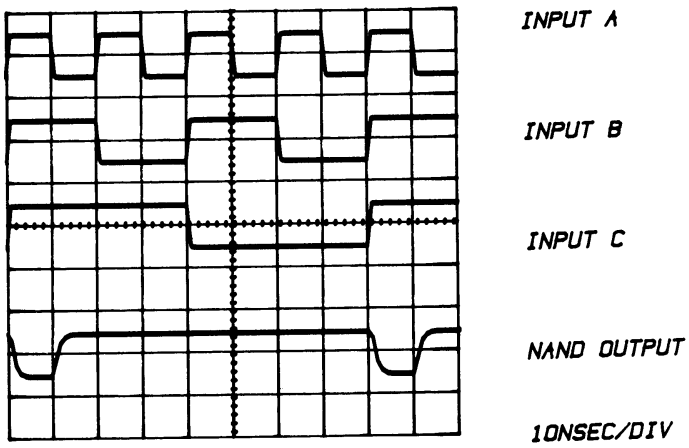

Figure 4, 3 input NAND gate simulation

Next, the nand gates were connected within a subcircuit to make a D Flip Flop. The PRE_SPICE parameter passing capability was used for initialization, as shown in the following listing.

TABLE 3, PRE_SPICE listing for a type D flip flop

```
DFLOP TEST
.OPTIONS ACCT
.TRAN 1NS 100NS
.PRINT TRAN V(1) V(2) V(3) V(4) V(5) V(6)
VCLK 3 0 PULSE 0 1 0 1NS 1NS 9NS 20NS
VCLR 1 0 PULSE 1 0 0 1NS 1NS 7NS 100NS VONE 4 0 1
X10 1 6 3 4 5 6 DFLOP
.SUBCKT DFLOP 1 2 3 4 5 6
X1 4 12 11 13 NAND3 {IC = 0}
X2 13 1 3 11 NAND3 {IC = 1}
X3 11 3 12 10 NAND3 {IC = 0}
X4 10 1 2 12 NAND3 {IC = 1}
X5 4 11 6 5 NAND3 {IC = 0}
X6 5 1 10 6 NAND3 {IC = 1}
.ENDS
*INCLUDE THRESH.LIB
.END
```

This circuit performed properly, much to our delight, so the next job was to check operation at yet another level. A three stage Johnson counter was simulated using the D Flip Flops and the results are shown in the following figure.

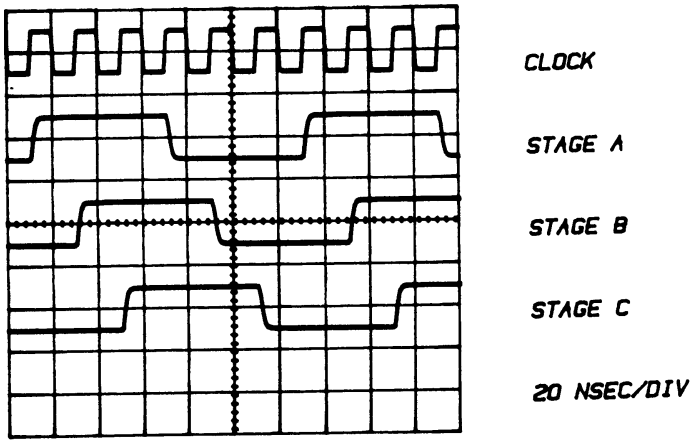

Figure 5, Johnson counter using threshold logic

When compared to a simple NMOS equivalent, the threshold version used about one half the memory and ran about 20% faster. The speed performance was somewhat disappointing and, was improved about 40% using the fifth order polynomial function shown in figure 3. The output was "noisier" but the circuit functioned properly.

METAL OXIDE TRANSISTOR GATE CAPACITANCE: The gate capacitance model for the built-in IS_SPICE model does not provide accurate results for power devices. The gate-drain capacitance is modeled as a constant. One must choose a compromise value or add a nonlinear capacitor. Lauritzen and Shi (1) provide an excellent discussion and a reasonable solution for this problem.

The nonlinear gate capacitance model causes a more realistic model for turn-off delay as shown in figure 6 for an IRF150 with a resistive drain load. The test circuit used a 10 Ohm gate drive and a 10 Amp drain resistive load.

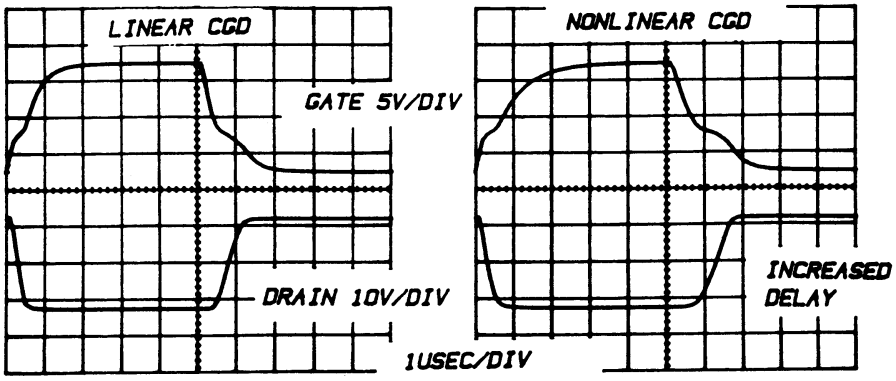

Figure 6, A nonlinear Gate-Drain capacitor improves switching response.

The gate drain capacitor was modeled by substituting the following subcircuit for CGDO in the FET model.

```
.SUBCKT CGD 1 2
VH 1 3 100
CGD 3 2 POLY 150PF 0 0 0 0 0 2E-21
.ENDS
```

This representation uses a sixth order polynomial capacitor in series with a voltage souce to model the larger capacitance seen a low voltages.

The new model was tested in the snubber circuit shown in the figure 7. The improved model was needed to prevent spurious device turn-on as shown in the accompanying analysis results.

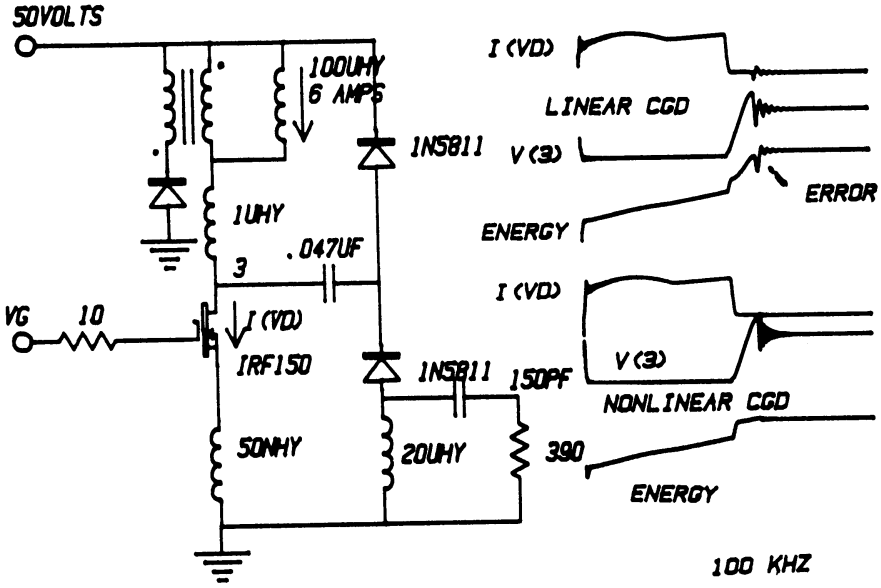

Figure 7, Lossless snubber, Waveforms show need for an improved power FET model.

Conclusion: The nonlinear gate-drain capacitance model is well worth adding to your power-FET models. This capacitance along with gate drive resistance and parasitic source inductance, are the most important parameters controlling power FET switching performance. If you are using the FET's for linear work you should modify the model slightly as discussed in this issues Cross-Talk column in order to run AC analysis.

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* * * * * CROSS TALK * * * * *

Cross talk is a regular feature of the Intusoft Newsletter in which frequently asked questions and problems are discussed.

Q. How many nodes can IS_SPICE handle?

A. IS_SPICE and mainframe SPICE use sparse matrix techniques to solve the matrix of equations that is used to represent the network. The memory required will therefore vary depending on the number and nature of branches. IS_SPICE reserves 160K bytes (40K 32 bit words or 20K double precision words) in a memory heap that is used for the matrix, to store the model and component values and the temporary output for an analysis. We have run a 300 node R-C chain which would require 300 x 300 double precision words or 4.5 times the memory allocation if sparse matrix techniques were not used. Other bench marks include a 200 node RTL inverter chain and 230 parallel bi-polar transistors (a 3 node circuit !!).

Q. Why does IS_SPICE complain about not having a DC path to ground?

A. When IS_SPICE solves for the initial operating point, inductors are shorted and capacitors are opened. If there were no DC path to ground, there would be a floating node which would cause a numerical singularity. All you have to do is place a large valued resistor across the offending capacitor or from the error flagged node to ground. Remember that these resistors can define the initial capacitor voltage, so that you may want to make them proportional to capacitance to effect charge division.

Q. I can't get a simple rectifier-capacitor circuit to run?

A. The simplest forms of this circuit will run, however, as circuit complexity increases the strong diode nonlinearity may cause convergence errors. These can be corrected by adding a large valued resistor (1E12 Ohms) across the diode or by modeling a reasonable value of capacitance in the diode model.

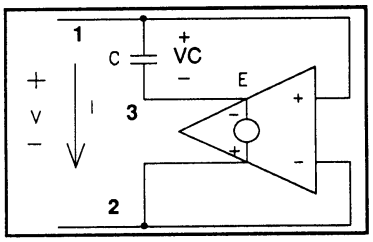
Q. How can subcircuits be initialized since the NODESET doesn't work in a subcircuit?

A. Neither IS_SPICE nor mainframe SPICE allow subcircuits to contain NODESET statements. If you include them, a warning will be issued and they will be ignored. The subcircuit will have to be initialized externally or by using initial conditions (IC = val) statements within the subcircuit. PRE_SPICE can be used to pass the initial conditions, creating new instance for subcircuits with different initial conditions.

See the application note on the D Flip Flop in this issue for passing IC's with PRE_SPICE. To pass nodesets from the main circuit, you will have to add test points so that the nodes you want to initialize are "visible" from the main circuit.

Q. How can Capacitor POLY functions be used in an AC analysis?

A. Neither capacitors nor inductors work properly in an AC analysis when the POLY keyword is used. This problem is common to both IS_SPICE and mainframe SPICE and a number of other versions. To solve this problem for capacitors, the following subcircuit can be used to make a voltage variable capacitor:



This circuit is described by the following:

$V = VC - E(V)$

$E(V) = Q0 + Q1*V + Q2*V^2 + ...$

$d(VC) = I/C\ dt = d(V + E(V))$

$C(V) = C*[1+Q1 + 2*Q2*V + 3*Q3*V^{2+....}]$

$= P0 + P1*V + P2*V^2$

Where P0,.... Pj are the polynomials that would be used in the capacitor POLY description and Q0,... Qj are used in the voltage controlled voltage source. Then

the capacitor description, C 1 2 POLY P0 P1 P2 .... is replaced by:
XC 1 2 POLYC {P0=val1 P1=val2 P2=val3 ... }

And the capacitor equivalent crcuit is built into the following subcircuit.

```
.SUBCKT POLYC 1 2
C 1 3 {P0}
E 2 3 1 2 0 0 {P1/(2*P0)} {P2/(3*P0)} {P3/(4*P0)} ....
.ENDS
```

Entries in curly braces must be replaced by their numerical evaluation before running IS_SPICE

Figure 7, A voltage variable capacitor for AC analysis

Q. How can the precision of the X-axis variable be improved in IS_SPICE?

A. The OPTIONS control statement will not affect the independent variable precision. If you specify something like an AC analysis with very small increments, then the frequency axis will report that all frequencies are identical. You will have to manually edit the output data or use Intu_Scope version 2.0 to make a new X Axis, subtracting the start frequency to improve resolution.

Q. Does IS_SPICE run on the new Compaq Deskpro 386?

A. Yes. So do the other programs. IS_SPICE runs about 2.7 times faster than on a PC AT.