Macromodels

Operational Amplifier Models

Operational Amplifiers, or Op-amps, can be modeled in a number of ways. The simplest op-amp is a voltage controlled voltage source which has the desired gain, while the most complex model uses the actual integrated or discrete circuit topology. The disadvantages of a complex model are that the analysis of a circuit with several amplifiers may use all the memory available in your computer, use excessive run time and require process information that the IC manufacturer holds proprietary. The simple model may not show important nonlinearities or other second order effects.

IsSpice4 accepts all commonly available vendor supplied op-amp and IC models.

Intusoft models are separated into libraries which represent two levels of complexity. The least complex models are good for a first cut analysis and require the smallest number of nodes. These models are in the LIN.LIB file. More complex models, in the NONLIN.LIB file, have more nodes. They require longer simulation time, while yielding a more complete description of the device. Refer to the Extended Syntax chapter of the IsSpice4 User's Guide to see how the different libraries can be included in your file.

The nonlinear models provided in NONLIN.LIB are hybrids. They duplicate part of the circuit topology to reproduce input and output nonlinearities, while simplifying the bias and interstage circuitry. Hybrid models are a compromise between the simple model and a complete simulation. The subcircuit

macro model which is used for op-amp simulation was developed by Intusoft. It is superior to the popular BOYLE op-amp model used by a number of SPICE model vendors. The Intusoft model solves a number of BOYLE model deficiencies, uses fewer components, is more easily adaptable to various op-amps, and simulates more efficiently and accurately.

Generic Op-amps

The Intusoft model libraries contain a number of models for commonly used op-amps. Other op-amp models are also available from various op-amp vendors. To obtain these models, contact Intusoft.

There are also several generic models. The generic models are equation-based subcircuit macros that can simulate hundreds of op-amps just by the specification of a few data sheet parameters. Generic models are possible because characteristics which are common to many op-amps can be modeled using similar techniques. There are generic models for op-amps that are constructed using bipolar and JFET technology, and for current feedback op-amps using 5 or 15 volts. These models are in the linear and nonlinear libraries. The library models for the generic op-amp subcircuits are called OPAMP (Bipolar front end), and FETAMP (JFET front end). The subcircuit names are the same in both libraries. This allows the designer to utilize either a complex or simple model just by altering the *INCLUDE statement. The current feedback op-amps are called AMPC5 (5 volt current feedback) and AMPC15 (15 volt current feedback) and are in the nonlinear library. Parameter passing is used to automatically calculate the IsSpice4 model parameters, based on the following list of commonly available data sheet parameters:

Data Sheet Value	Parameter
Bandwidth	FT
*Slew Rate Limit	DVDT
Bias Current	IBIAS
Offset Current	IOS
Offset Voltage	VOS
DC Gain	GAIN
*Bandwidth (-3dB)	FC
*Feedback Resistor	RF

* Used for current feedback op-amp

Example: XAMP 1 2 3 4 5 OPAMP {FT=5MEGHz DVDT=5E6 +IBIAS=1NA IOS=1NA VOS=200UV GAIN=150E3}

The nonlinear JFET front end model requires FT, DVDT, VOS, and GAIN. The linear JFET model requires the parameters FT, VOS, and GAIN, while the Bipolar model requires specification of FT, IOS, VOS, IBIAS, and GAIN. The op-amp connections in the order that they must be specified are: (-) inverting input, (+) non-inverting input, output, VCC (+ supply), and VEE (- supply). The current feedback op-amps require the parameters FC, DVDT and RF. The connections as they appear in the subcircuit netlist are: (-) inverting input, (+) non-inverting input, output, VCC (+ supply), and VEE (- supply). See the "SPICE APPLICATIONS HANDBOOK" for a detailed explanation of the current feedback op-amp.

Many other parameters could have been specified, however a lengthy parameter list would discourage use of the generic model. These models have a strong technology and circuit design dependence which constrains meaningful parameter values to be in the neighborhood of those found in vendor data sheets.

Besides modeling the linear and DC transfer function, the nonlinear generic model includes the following characteristics:

- Input Stage Nonlinearities
- Input Voltage and Current Offsets and Bias
- Slew Rate Limiting
- Common Mode Gain
- Power Supply Rejection
- Output Current Limiting
- Output Voltage Limiting
- Reflection of Load Current to Power Input
- Output Stage Nonlinearities

The equivalent circuit shown in Figure 1 takes advantage of the idealized device behavior which is possible through simulation. Parameters are defined for the three stages of the simulated amplifier.

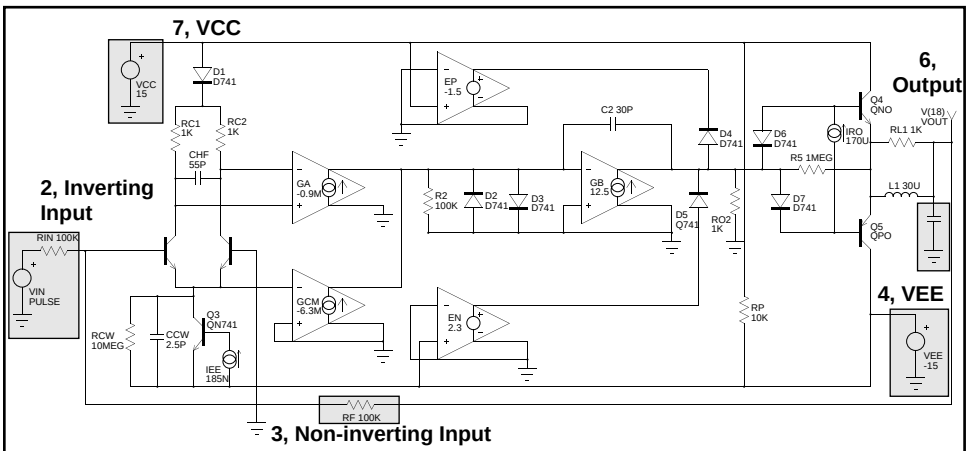

Figure 1, A generic nonlinear op-amp equivalent circuit; Shaded areas contain components which are external to the actual op-amp model and are used for simulation purposes only.

Input Stage

The input nonlinearities are simulated using Q1, Q2, Q3 and D1. These are setup to simulate the topology for a 741 or similar amplifier with respect to bias and common mode range. The input transistors, Q1 and Q2, should be modeled to reflect the performance characteristics of the op-amp so that bias current,

offset current and offset voltage are modeled. Noise parameters can also be modeled in this stage by changing the values for AF and KF in the input BJT model QNI1. RCM and CCM will convert common mode signals to differential signals and also couple power line variations into the input. The high frequency pole is modeled with RC1, RC2 and CHF. Values of RC1 and RC2 must be small in order to get the input capacitance of Q1 and Q2 to provide reasonable high frequency behavior. Q1 and Q2 are made slightly different to develop input offsets, and their emission coefficients can be selected to simulate the effect of other transistor cascades in the input and slew rate limiting.

Slew rate limiting is set by this input stage. The large signal output voltage is limited to BETA3 * IEE * RC and the small signal gain is RC * .5 * BETA3 * IEE / (N * VT). If the small signal output is integrated to provide a unity gain crossover at the radian frequency, WT, then the slew rate is:

$$\text{Slew Rate, } \frac{dV}{dt} = 2 * N * VT * WT \qquad \text{Eq. 7.1}$$

The emission coefficient, N, then sets the slew rate limit. Alternatively, you could add emitter resistance as is done in some other models, however, modifying N uses fewer nodes. To make the slew limit unsymmetrical, you can unbalance the collector resistances RC1 and RC2. Note that slew rate limiting is closely related to physical parameters and front end topology as shown in equation 7.3. The emission coefficient of the front end is used to control bandwidth, while bias current controls the slew rate. Slew rate should be within an order of magnitude of the FT to prevent unusual circuit behavior.

Interstage

Controlled sources GA and GCM couple the differential and common mode signals to the interstage amplifier, GB. The DC gain is given by:

$$\text{Adiff} = RC*0.5*\left(\frac{BETA3*IEE}{N*VT}\right)*GA*R2*GB*RO2 \qquad \text{Eq. 7.2}$$

At frequencies below the pole at W = 1/(2 ∗ RC ∗ CHF), the gain is given by:

$$\text{Adiff(mid freq.)} = RC*0.5*\left(\frac{BETA3*IEE}{N*VT}\right)*\frac{GA}{jW*C2} \qquad \text{Eq. 7.3}$$

and the unity gain frequency is approximated by solving for W when Adiff = 1.

Two nonlinearities are modeled in the interstage. First, the large signal overshoot is limited by diodes D2 and D3. For amplifiers where this is caused by a pair of diodes, the emission coefficients of the diodes can be adjusted. The second nonlinearity is the output swing which is taken as a constant value subtracted from the power rails. D4, D5, EP and EN act as output limiters. It is important to return the limited current to the subcircuit ground node so that the source, GB, does not generate any apparent power. Static power dissipation is modeled using the resistor RP connected across the power lines.

Output Stage

The output stage is modeled using D6, D7, Q4, Q5 and L. The transistors are not given any AC parameters. Instead, a discrete inductor simulates the AC performance while the transistors' (QNO and QPO) BETA and the source IRO account for both current limit and output resistance. This stage will return the load current to the power lines, enabling simulation of certain power stage configurations.

Example Bipolar and JFET Input Op-amps

The 741 op-amp is a high performance monolithic operational amplifier which is used in many of today's electronic products. Fairchild first developed the UA741; the most comprehensive data sheets may be found in the Fairchild Linear Products catalog.

This amplifier model is based on the generic op-amp model. Models are in the LIN.LIB and NONLIN.LIB files. The linear model is shown in Figure 2.

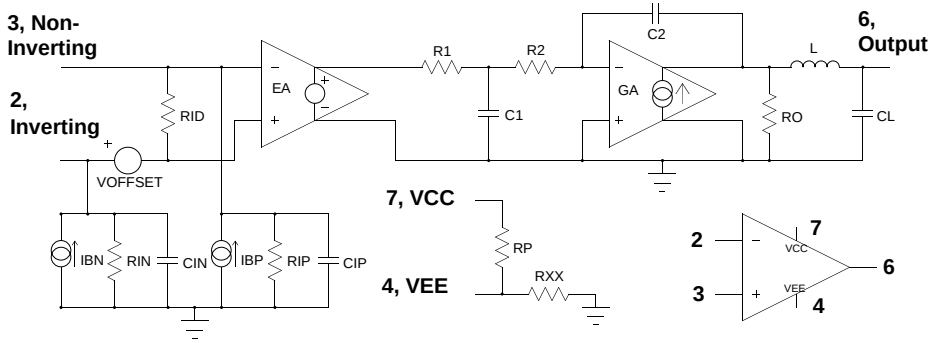

Figure 2, The UA741 equivalent circuit using the Intusoft linear model. On the right is the SPICENET symbol which shows connectivity.

The 156 op-amp was first developed at National Semiconductor under the part number LF156, and features a high impedance JFET front end with relatively fast slew rate and high gain-bandwidth product. The low bias current makes it possible to eliminate bias current compensation resistors; however, its higher bandwidth requires extra care in layout.

Figure 3 defines the topology, and the LIN.LIB and NONLIN.LIB files contain the subcircuit models.

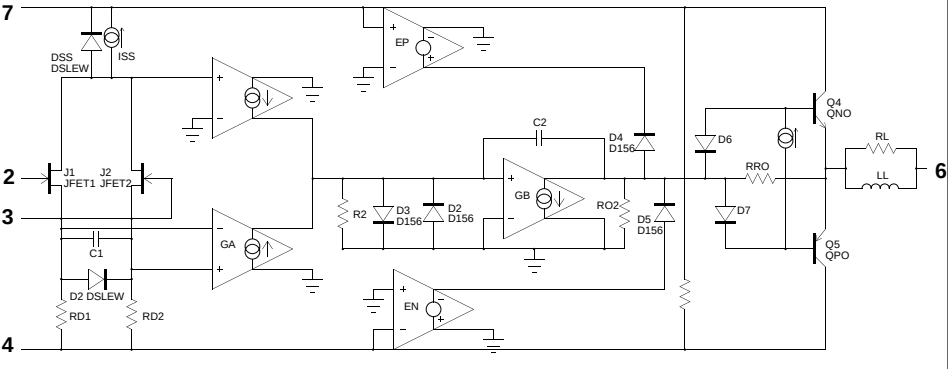

Figure 3, The LF156 equivalent circuit using the Intusoft nonlinear op-amp model.