Personal Computer
Circuit Design
Tools

Working with Model Libraries

One Civic Plaza Dr., Suite 470
Carson, CA 90745
Tel. 310-952-0657
Fax 310-952-5468
email info@intusoft.com
web - www.intusoft.com

IsSpice4 is based on Berkeley SPICE 3F.5, which was developed by the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley CA and XSPICE, which was developed by Georgia Tech Research Corp., Georgia Institute of Technology, Atlanta Georgia, 30332-0800

Portions of IsSpice4 have been developed at Universite Catholique de Louvain in Belgium, University of Illinois, and Macquarie University in Australia. Many thanks to Benjamin Iniguez, Pablo Menu, Anthony Parker and Christophe Basso for their contributions to IsSpice4 's models. Portions of this manual have been previously published in EDN Magazine.

SpiceMod sections of this manual are provided and apply only if you have purchased an ICAP/4Windows Deluxe, ICAP/4Windows Professional, Power Supply Designer or Test Designer program.

This publication may contain technical inaccuracies or typographical errors. Changes are periodically made to the information herein; these changes will be incorporated in new editions of this publication.

is a trademark of ***intusoft***

Printed in the U.S.A. rev. 12/08

Contents

TABLE OF CONTENTS

Chapter 8 SpiceMod Installation and Introduction

Chapter 9 Quick Start Tutorial

Chapter 10 Program Operation

TABLE OF CONTENTS

Chapter 1 - Modeling Semiconductors

Introduction

Designing circuits using computer simulation requires that models accurately reflect device behavior within a specific circuit context. Models with excessive detail will obscure the circuit designer's insight and will quickly reach both run-time and complexity limitations of the simulation program. Overly simple models will fail to predict key circuit performance parameters and may lead to costly design mistakes.

Device modeling is one of the most difficult steps in the circuit simulation process. It requires not only an understanding of the device's physical and electrical properties, but also an intimate knowledge of the particular circuit application. Each IsSpice4 primitive element carries with it a list of parameters which effect its behavior. A great deal of practice and experience is needed in order to know which parameters are important and when.

Nevertheless, the problems of device modeling are not insurmountable and a good first cut model can be made quickly, giving the designer an accurate device model for a wide range of applications.

The level of detail that is used in a design task begins with the simplest model to test various concepts. Models then become progressively more complex as the design is re-

fined. The simulation must be tested by comparing results with experience and real hardware performance. An experienced designer can ferret out the simulation errors with very little laboratory verification, while the novice should test the design at each step. These tests do not have to be based on first-hand laboratory data. Frequently, it is possible to compare simulation results with published data found in vendor data sheets, magazine articles, and other designer's handbooks.

Data sheet information is generally conservative, yet it provides information which is useful for a good first cut at a device model. Laboratory measurements and methods for gathering data from test setups is beyond the scope of this guide, and will not be covered except in a few passing notes. However, a test setup which provides data similar to that supplied by a data sheet will be applicable to the methods discussed.

IsSpice4 models have default values that produce reasonable first order predictions. More complex models can be created either by supplying additional model parameters for the built-in models or by creating subcircuits that represent analogs of the device. A capacitor, for example, could be represented as a simple capacitance value for the first cut of an analysis. Later on, it could be replaced by a subcircuit which contains parasitic inductance, series and parallel resistance, and nonlinear voltage coefficients for a more detailed model.

To model more complex electronic devices, such as operational amplifiers, it is best to use the basic set of IsSpice4 primitives in a subcircuit. This type of modeling is called macro modeling. It is well suited to the electrical engineer because it produces a behavioral model which is understood by circuit designers, rather than forcing the designer to learn a new programming language.

The chapters that follow will get you going in the right direction. They contain a review of the majority of the parameters which are associated with the diode, bipolar transistor, JFET, MOSFET and other electrical components, and example modeling sessions. They also contain numerous macro models and explain how they were developed and how to use them.

Diodes

Syntax: DNAME Anode Cathode Modelname <OFF> <IC=VD>

Example: DRECT 1 2 DN4148
.MODEL DN4148 D(RS=.8 CJO=4PF IS=7E-09
+N=2 VJ=.6V TT=6E-09 M=.45 BV=100V)

The diode is the most fundamental semiconductor element. An understanding of its parameters and their effects can be further extended to the transistor models. Applicable to both junction diodes and Schottky barrier diodes, the equivalent circuit shown in Figure 1 describes the IsSpice4 diode model.

The behavior of the IsSpice4 diode relies heavily on a prescribed set of parameters. These parameters govern the overall characteristics of the model. Some of the parameters are available from manufacturer's data sheets, while others must be calculated or measured in the laboratory. Virtually all of the parameters come into play when modeling the diode.

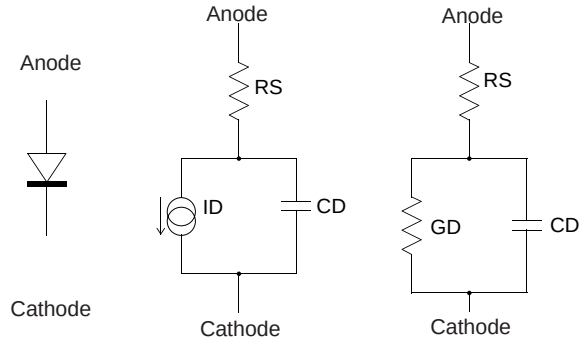


Figure 1, IsSpice4 uses these circuits to model the diode for large signal transient and small signal analyses.

IsSpice4 does not supply defaults for dynamic parameters. For reasonable simulation results, the capacitance parameters CJO, VJ, and M should be specified. Generally speaking, if the diode model reflects the actual device, convergence performance will be good. Diodes which are used in switching applications must also specify TT, the transit time parameter.

Default Diode Limitations

There are 3 regions where the default diode characteristic differs from the real life response. These differences are described by the I/V curves given on the following page.

Turn On region: where the carrier generation/recombination in the space charge layer affects behavior. The default diode will turn on as soon as it is forward biased.

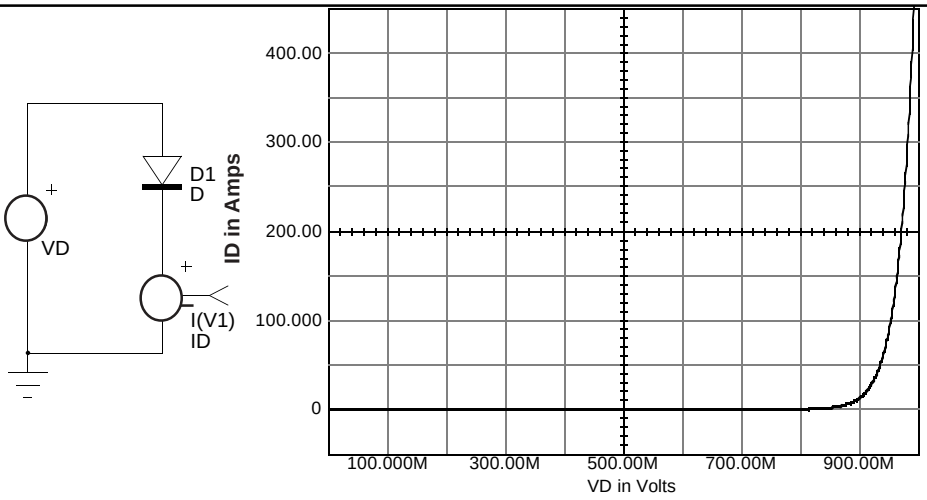


Figure 2, The diode characteristic I/V curve using IsSPICE4 model defaults.

High level injection region: due to series resistance. The default diode curve will not bend at higher voltages; current will increase linearly with voltage.

Breakdown region: due to internal breakdown associated with high reverse voltage. The default diode will not breakdown at any value of reverse voltage.

Additionally, junction capacitance (CJO), and transit time (TT) are zero.

Other Diode Model Limitations

The IsSPICE4 diode model gives good results in most applications; however, the following parameters are not accurately modeled:

Reverse breakdown temperature coefficient.

Reverse recovery variations due to junction grading such as in step recovery diodes.

Forward recovery time

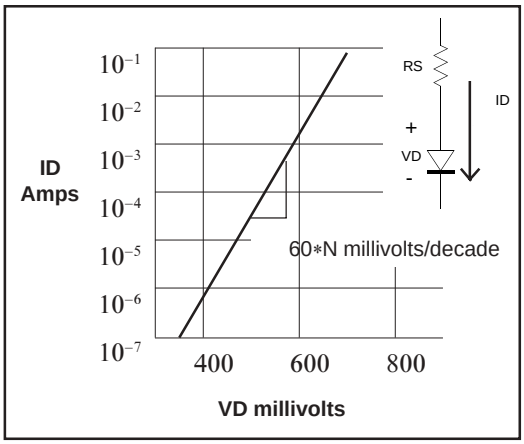
Thermal feedback that causes junction temperature to change as a function of power dissipation.

Notes About Using The Default Diode Model

Avoid using the default diode model; it can cause a variety of convergence problems due to the diode's strong nonlinearity in the turn-on region. As a rule, a diode model should always have a value for the junction capacitance, “CJO”.

Diode leakage can be simulated by placing a large-valued resistor (100 megohms) across the diode. This will also help alleviate convergence problems.

Forward Conduction



The foundation of the diode model is the diode equation (Eq. 1.1) which describes conduction in the forward direction (usually LOG ID vs. VD on most data sheets). This data yields three important IsSpice4 parameters, N, IS, and RS.

$$ID = IS\left(e^{\frac{VD}{N*VT}} - 1\right)$$ Eq. 1.1

where: VT = Thermal voltage
= K ∗ T / q, .026 Volts at room temperature, 27 °C

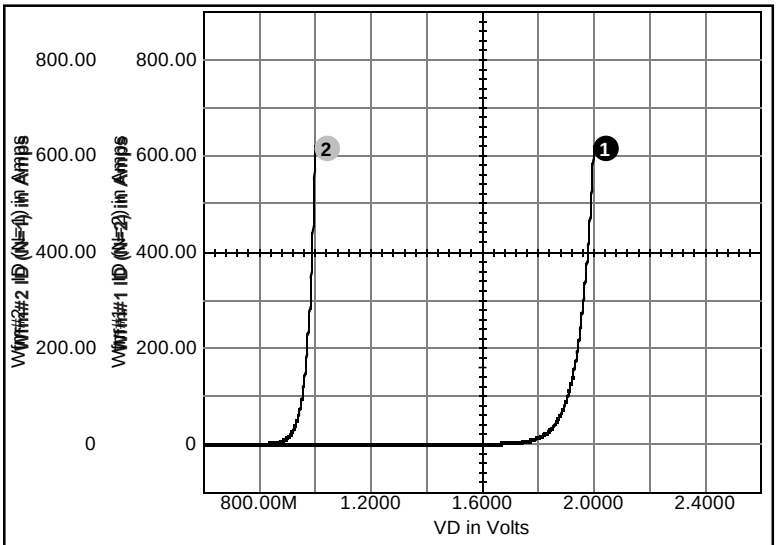


Figure 3, I/V characteristics using different emission coefficients.

IS and N are ISSPICE4 model parameters.

N: Emission coefficient, default = 1

The emission coefficient controls the slope of the I/V curve, especially in the high injection region. The emission coefficient is 1 when diffusion current dominates and 2 when recombination current dominates and for high injection. The default value of N is good for most integrated circuits; however, most discrete devices have N values which are nearer to 2. Measuring the change in diode voltage for several decade changes in current will yield 60 mv/decade if N is unity, and 120 mv/decade if N is 2. This is equivalent to plotting LOG(ID) vs VD and measuring the slope in the linear region.

The basic diode equation gives gross first order I/V characteristics. In circuits where the details of the diode response are important for proper operation, additional model parameters must be included to simulate second order effects.

IS: Saturation current, default=1E-14

The reverse saturation current, IS, is the amount of current an ideal diode will conduct over a large range of reverse bias voltage. IS is determined from ID vs. VD measurements with the diode forward biased. Determination of IS using reverse biased measurements is discouraged because parasitic leakage is generally much larger than IS. IS should be calculated in the forward biased region where the plot of log(ID) vs. VD is a straight line. Note that IS must be increased exponentially as the emission coefficient, N, is increased in order to maintain the same operating point.

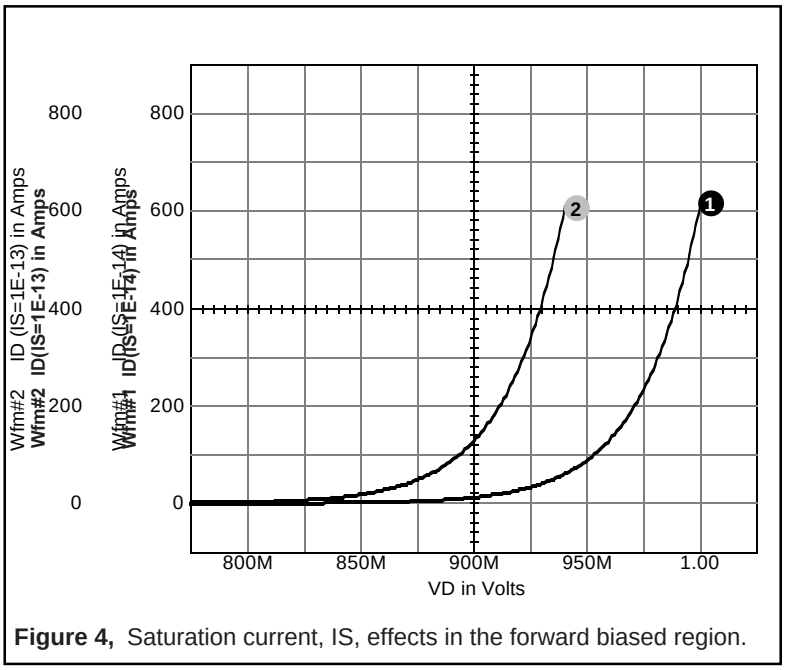


Figure 4, Saturation current, IS, effects in the forward biased region.

RS: Series resistance, default=0

Series resistance is used to model both the ohmic resistance and the diode transition to the high injection region. RS accounts for the diode deviation from ideal voltage predicted from IS and N at high bias levels. It may be determined from two points on the forward current (LOG ID) vs. voltage (VD) curve at high current levels. One point is chosen directly on the I/V

curve. The second point is located at the intersection of the first points' current level and the extrapolation of the straight line portion of the curve. Both points should have the same current level, but different voltage values. The voltage difference divided by the current is the series resistance:

$$RS = \frac{(VD1 - VD2)}{ID} \qquad \text{Eq. 1.2}$$

Typical values for RS are less than 1 ohm.

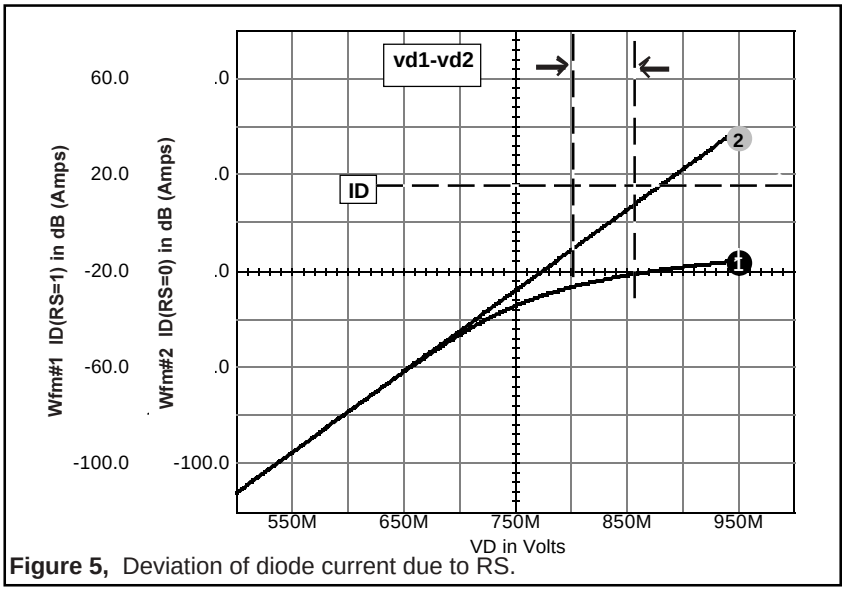
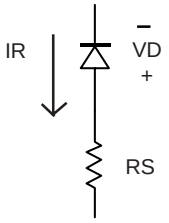


Figure 5, Deviation of diode current due to RS.

Diode Reverse Conduction



Conduction in the reverse direction is governed by the breakdown voltage, BV, and the current at breakdown, IBV, according to the following equation:

$$IR = IBV * e\left(\frac{(-VD - BV)}{VT}\right) \qquad \text{Eq. 1.3}$$

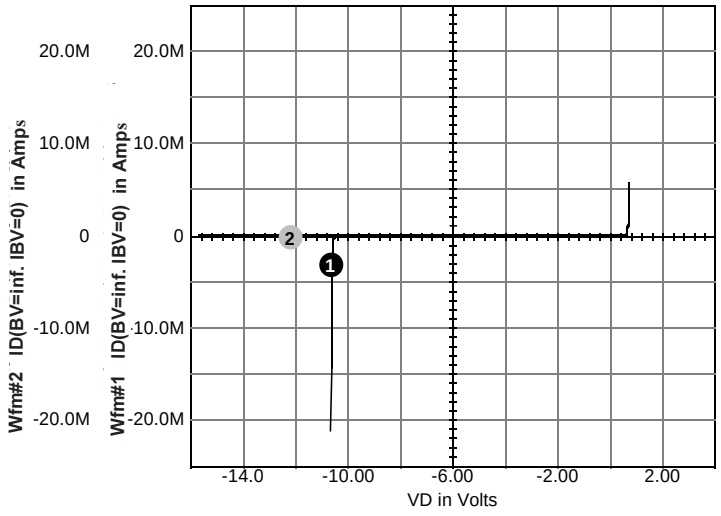


Figure 6, Including BV and IBV yields familiar reverse voltage behavior.

BV: Breakdown Voltage, default=infinity
IBV: Current at Breakdown, default=0

If reverse data is available, BV and IBV can be estimated using a piece-wise linear best-fit line. Data sheets usually give minimum values for breakdown voltage; typical breakdown is generally 50% higher. Measurements of these parameters are not recommended for breakdown ratings above several hundred volts because of the danger of damaging the device by arcing across the surface.

Diode Charge Storage

Parameters CJO, VJ, M, and FC model charge storage in the junction depletion region and can be obtained from capacitance bridge measurements at several values of reverse bias, or from data sheet curves. The values for CJO are usually in the picofarad range for normal PN diodes, but may be in the nanofarad range for larger power diodes. Experience with

IsSPICE4 has shown that using a reasonable value for CJO will substantially improve convergence in transient simulations.

CJO: Zero Bias Junction Capacitance, default = 0
VJ: Junction Potential, default = 1V
M: Grading Coefficient, default = 0.5
FC Coefficient for Forward Bias Depletion Capacitance, default = 0.5

It is recommended that a CJO value of at least 2 PF is used in all discrete diode models. Typically, VJ varies between 0.2 and 1Volt and M ranges from 0.3 for a linearly graded junction to 0.5 for an abrupt junction. FC determines how the forward biased depletion capacitance will be calculated. Reverse bias capacitance is given by the equation:

$$CD = CJO * \left(1 - \frac{VD}{VJ}\right)^{-M} \qquad \text{Eq. 1.4}$$

Forward bias capacitance reverts to:

$$CD = CJO * (1 - FC)^{-(1-M)} * \left(1FC * (1 + M) + M * \frac{VD}{VJ}\right)$$

when $VD > FC * VJ$ Eq. 1.5

Charge storage due to minority carrier injection is given by:

$$QS = TT * IS\left(e^{\frac{VD}{N*VT}} - 1\right) \qquad \text{Eq. 1.6}$$

and is estimated from pulsed delay time data or measurement in order to find the parameter TT. Notice that the measurement will also include the contribution from CJO.

TT: Transit Time, default=0

When a forward biased diode is abruptly reverse biased, there is a discrete amount of time which elapses before the diode is no longer conducting. This amount of time is called the reverse recovery time, (TRR). A large part of the recovery time is the device storage time. Storage time is normally provided by vendors for switching type diodes.

TT can be computed from the diode storage time, TS, using the following equation:

$$TT = \frac{Ts}{\ln\left[1 + \frac{IF}{IR}\right]} \qquad \text{Eq. 1.7}$$

where IF is the forward current and IR is the reverse current.

Variation With Temperature

There are four diode parameters that are modified in IsSPICE4 to reflect changes in temperature. They are IS, VJ, CJO, and FC. The saturation current, IS, causes the greatest effect upon temperature dependence.

Temperature Coefficient: The temperature dependence of saturation current, IS, is proportional to:

$$IS\left(T_{NEW}\right) = IS\left(T_{NOM}\right) * T\frac{XTI}{N} * e^{\left[\left(\frac{-q*EG}{N*k*T_{NEW}}\right)*(1-T)\right]}$$

where $T = \frac{T_{NEW}}{T_{OLD}}$ Eq. 1.8

EG : Energy Gap , default = 1.11eV
XTI : Saturation current temperature exponent, default = 3.0

The parameters XTI and EG will describe the saturation current behavior as a function of temperature when temperature, T, is varied from the nominal. Representations which are more accurate than the default are unnecessary unless different materials, for example, Gallium Arsenide, are used or if more exact temperature behavior is needed to model circuits such as a bandgap reference.

Typical values for XTI are 3 for a PN diode, and 2 for a Schottky diode. Values for EG at room temperature are 1.11 for a PN diode and 0.69 for a Schottky diode.

Note that IsSPICE4 can only simulate a circuit at one temperature at a time. The default temperature is 27 degrees. To change the temperature, use the .TEMP command. It is possible using advanced modeling techniques to create an analog of temperature in an analysis and thus have temperature become a variable.

Diode Noise

KF: Flicker noise coefficient, default = 0
AF: Flicker noise exponent, default = 1

Shot and flicker noise are modeled as:

$$ID^2 = \left(2 * q * ID + \frac{(KF * ID^{AF}}{f}\right) * \left(D_f\right) \qquad \text{Eq. 1.9}$$

Thermal noise is modeled as:

$$I_{RS} = \frac{4kT}{RS} * \left(D_f\right) \qquad \text{Eq. 1.10}$$

Diode noise is not significant for most circuits, however, the diodes associated with transistors behave in a similar fashion and are responsible for most noise associated with electronic circuits. The typical values for KF and AF are 10^{-16} and 1, respectively, for silicon diodes.

Area Dependence

The area factor in the diode call statement determines the number of equivalent parallel devices which will be created. The area parameter affects IS, RS, and CJO.

Example of Modeling From A Data Sheet

When possible, data extraction from the manufacturer's data sheet is recommended since this data is a mean over a large number of components, and will be able to yield either a MIN, MAX, or typical model. Laboratory measurements can also be made in order to verify model accuracy. The data in Figure 8 is typical of that provided in a vendor data sheet for a 1N4001 rectifier diode. Remember, when modeling a component, that initial guesses or calculations of parameters may need to be tweaked. After simulating, the newly created model parameters may be adjusted accordingly to provide a superior fit to the data sheet curves.

Designers Data Sheet

***MAXIMUM RATINGS**

Rating	Symbol	1N4001	1N4002	1N4003	1N4004	1N4005	1N4006	1N4007	Unit
Peak Reptitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	50	100	200	400	600	800	1000	Volts
Non-Reptitive Peak Reverse Voltage (halfwave, single phase, 60 Hz)	V_{RSM}	60	120	240	480	720	1000	1200	Volts
RMS Reverse Voltage	$V_{R(RMS)}$	35	70	140	280	420	560	700	Volts
Average Rectified Forward Current (single phase, resistive load 60Hz, see Figure 8, T_A = 75 deg C)	I_O	1.0						Amp	
Non-Repetitive Peak Surge Current (surge applied at rated load conditions, see Figure 2)	I_{FSM}	30 (for 1 cycle)						Amp	
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +175						deg C	

***ELECTRICAL CHARACTERISTICS**

Characteristic and Conditions	Symbol	Typ	Max	Unit
Maximum Instantaneous Forward Voltage Drop (I_F = 1.0 amp, T_J = 25 deg C) Figure 1	VF	0.93	1.1	Volts
Maximum Full-Cycle Average Forward Voltage Drop (I_O=1.0 amp T_L=75 deg C, 1 inch leads)	$V_{F(AV)}$	--	0.8	Volts
Maximum Reverse Current (rated dc voltage) T_J = 25 deg C T_J = 100 deg C	I_R	0.05 1.0	10 60	uA
Maximum Full-Cycle Average Reverse Current (I_O=1.0 amp, T_L= 75 deg C, 1 inch leads)	$I_{R(AV)}$		30	uA

Figure 8, Typical data sheet for the 1N400X rectifier diodes

Determination of Parameters From Data Sheets

As you look through vendor data sheets, you will notice that some diodes have plots of LOG(ID) vs VD, and some do not. Generally speaking, the vendor that first registered the JEDEC part will provide the necessary data. Unfortunately, the data is sometimes omitted in later catalogues, so you must either make measurements or dig up the old data sheets. Frequently, the data sheet specification is loose enough for different vendors to have considerable margin in part fabrication, so be careful!

Data sheets usually give average measurements of device performance. Depending on the application, one or more parameters could be changed to investigate worst-case performance. In a diode model, changing the value of IS, RS, or TT will provide real life performance variations.

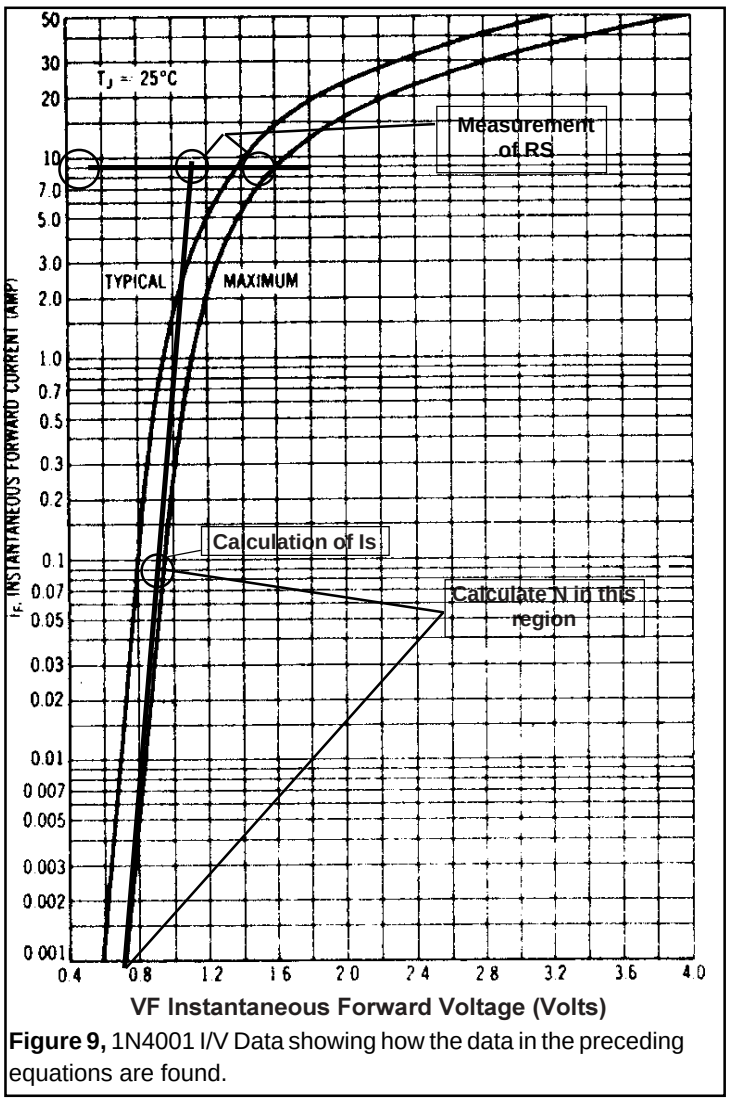


Figure 9, 1N4001 I/V Data showing how the data in the preceding equations are found.

The emission coefficient, N, is computed by measuring the slope of the LOG(ID) vs VD curve from Figure 9.

$$N = \frac{VD1 - VD2}{\left(2.3 * VT * \log\left(\frac{ID2}{ID1}\right)\right)} = 1.7 \qquad \text{Eq. 1.11}$$

RS is computed at ID = 10 Amps by taking the voltage deviation, .4 volts, along the straight line shown on Figure 9.

$$RS = \frac{(V2 - V1)}{I} = \frac{0.4V}{10A} = 0.04\Omega \qquad \text{Eq. 1.12}$$

IS can be computed anywhere along the straight line portion of the curve.

$$IS = \frac{ID}{e^{\left(\frac{VD}{N*VT}\right)}} = \frac{0.1A}{e^{\left(\frac{0.8V}{1.7*0.026}\right)}} = 1.38E-9 \qquad \text{Eq. 1.13}$$

Breakdown voltage and current are typically:

$$BV = 75VA \text{ AND } IBV = 0.05\mu A$$

The junction capacitance parameters, M, CJO, and VJ are computed from the reverse bias C-V curve. A best-fit line, shown in Figure 10 above the two curves, is used to compute M. VJ should be small compared to VD over the region of the

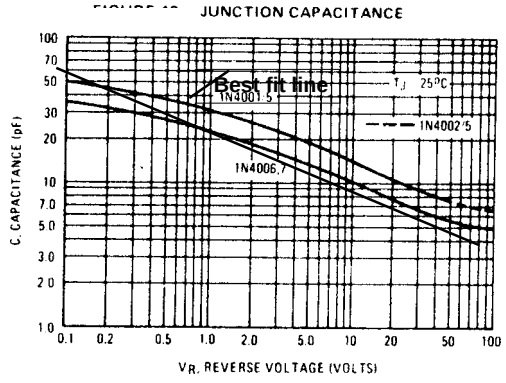


Figure 10, 1N4001 data for junction capacitance

best-fit. Using (100P,0.1V) and (7P,100V);

$$M = \frac{\log\left(\frac{C1}{C2}\right)}{\log\left(\frac{V2}{V1}\right)} = \frac{\log\left(\frac{100\ p}{7\ p}\right)}{3} = 0.38 \qquad \text{Eq.1.14}$$

Next, VJ is computed using 2 data points, one of which is near VD = 0. Using (50p,0.1V) and (15p,10V);

$$VJ = \frac{\left(V2 * \left(\frac{C1}{C2}\right)^{-\frac{1}{M}} - V1\right)}{\left(1 - \left(\frac{C1}{C2}\right)^{-\frac{1}{M}}\right)} = \frac{\left(10 * \left(\frac{50}{15}\right)^{-2.63} - 0.1\right)}{(1 - 0.4215)} = 0.34\,V \qquad \text{Eq. 1.15}$$

Finally, CJO is computed at one of the points (50p,0.1V).

$$CJO = \frac{C1}{\left(\left(1 + \frac{V1}{VJ}\right)^{-M}\right)} = \frac{50\,p}{\left(1.294^{-0.38}\right)} = 55\,p \qquad \text{Eq. 1.16}$$

The built-in voltage, VJ, is not within the region predicted by the device's physical properties. Remember that the diode equation is a simplified representation of the semiconductor's physics and that fitting experimental data may result in unusual values. Radical departures should be confirmed via testing.

Diode reverse recovery time is a combination of transit time and depletion region charge removal, and is usually dominated by the transit time parameter. Using IR/IF = 1 from the data sheet gives a recovery time of 3.5USEC for IF = .1 to 1 Amps. When the diode current reverses polarity, charge is removed from the diode terminals as a linear function of time, and minority carrier recombination reduces the stored charge with the time constant, TT. When forward current equals reverse current, the transit time, TT is 1.44 * TS, the diode storage time. For the 1N4001,

$$TT = 1.44 * 3.5\mu s = 5\mu s \qquad \text{Eq. 1.17}$$

Figure 11, Reverse Recovery Time

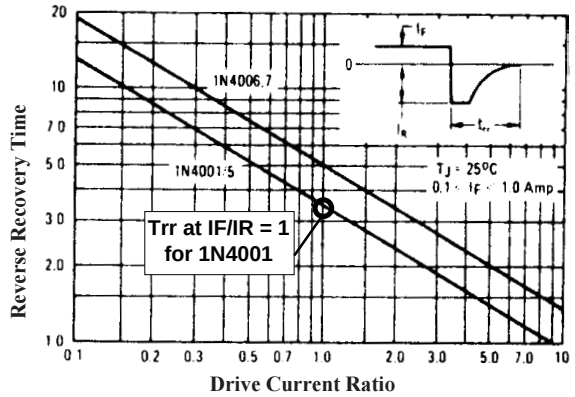


Figure 11, Using the 1N4001 reverse recovery data, choose a typical point for your application, then use trr and Eq. 2.17 for TT.

Generic Diodes

Modeling diodes is not always easy. Manufacturers rarely give junction capacitance values, and some don't even give forward conduction characteristics. The generic diode lets you create a model simply by providing maximum current (IMAX), maximum voltage (VMAX) and a reverse recovery time (TRR) parameter.

The generic model can be found in the DEVICE.LIB file. The concept of a generic component is simple. Using simple approximations based on semiconductor physics and basic principles surrounding the fabrication of semiconductors, it is possible to construct a model for a diode that is a function of data sheet parameters. Though usually incomplete, data sheet parameters can be converted into IsSpice4 parameters. There are 14 IsSpice4 diode parameters, 9 of which have unacceptable defaults. The model below uses data sheet parameters to alter these defaults and create a reasonable model.

Syntax: XNAME 1 2 DIODE {IMAX=# VMAX=# TRR=#}
Example: XD1 2 5 DIODE {IMAX=3 VMAX=100 TRR=3N}

Forward characteristics and capacitance are estimated from the parameters IMAX, VMAX, and TRR. Reverse recovery time is relatively independent of the current and voltage characteristics, and must be specified explicitly. If reverse recovery time is not given, you can assume that the diode is slow and use a value of 5 USEC. Junction capacitance is proportional to area, which is also proportional to current-carrying capability, IMAX. Breakdown voltage, storage time and manufacturing process also control capacitance. Unfortunately, the manufacturing process has a stronger influence than other electrical parameters, so the best estimate for CJO is IMAX. Actual capacitance data, either from measurements or the data sheet, is preferable to the default calculation which is based on IMAX values. Ohmic resistance increases with breakdown voltage, however, the vendor current and voltage specifications take this into account. IMAX will usually signal an increase in forward voltage over the ideal diode by .075 volts. The generic model will generally be within the range permitted by the JEDEC specification. Our usual caveat about designing with unspecified parameters applies; however, with diodes we take our chances! The following equations are used in the generic model:

```
CJO = 30P * IMAX
IS = 5N * IMAX
TT = 1.44 * TRR
BV = 1.5 * VMAX                    EQ. 1.18
IBV = 1UA
N = 2
M = .5
VJ = 1
RS = .075 / IMAX
```

The subcircuit is listed in the library as follows:

```
*********************************************
GENERIC DIODE, PARAMS ARE IMAX,TRR,VMAX
.SUBCKT DIODE 1 2
D1 1 2 DIODE
.MODEL DIODE D(CJO={30P*IMAX} IS={5N*IMAX} +TT={1.44*TRR}
+ BV={1.5*VMAX} IBV=1UA N=2 RS={.075/IMAX})
.ENDS
*********************************************
```

The generic model uses the parameter passing feature to pass parameters from the subcircuit call line “X” into the subcircuit. To use the generic subcircuit model, call the subcircuit with the proper command line extensions.

For example, placing the following line in your netlist will call the generic diode subcircuit and pass the IMAX, TRR, and VMAX parameters into the subcircuit. The parameters below are from a 1N4001 data sheet.

```
X1 5 6 DIODE {IMAX=1 TRR=3.5U VMAX=35}
```

Param will then evaluate the expressions that are in curly braces using the passed parameters, and then replace the expressions with numbers. The following subcircuit netlist will result:

```
.SUBCKT DIODE 1 2
D1 1 2 DIODE
.MODEL DIODE D(CJO=30.000P  IS=5.0000N  TT=5.0400U
+ BV=52.500   IBV=1UA  N=2  RS=75.000M)
.ENDS
```

Recalling our earlier study of modeling, the 1N4001 diode model looks something like this:

```
.MODEL DN4001 D(N=1.7 RS=0.04 IS=1.38E-9 BV=75
IBV=.05U +M=.38 VJ=.34 CJO=55PF TT=5U)
```

For comparison, a simulation of forward bias current versus voltage for both models is shown in the graph below. You will notice that the derived model has a bit more current at the same level of voltage bias. Careful examination of both models reveals that all the parameters except for RS are quite close. The parameter RS will have an effect on the data you see in the figure. Referring back to Figure 9, the actual data predicts that the current should be around 10 amps for a forward voltage of 1.5. The generic model is not far off at about 6 amps, and provides an excellent model quickly and easily without complex calculations. The generic calculation for RS is conservative and

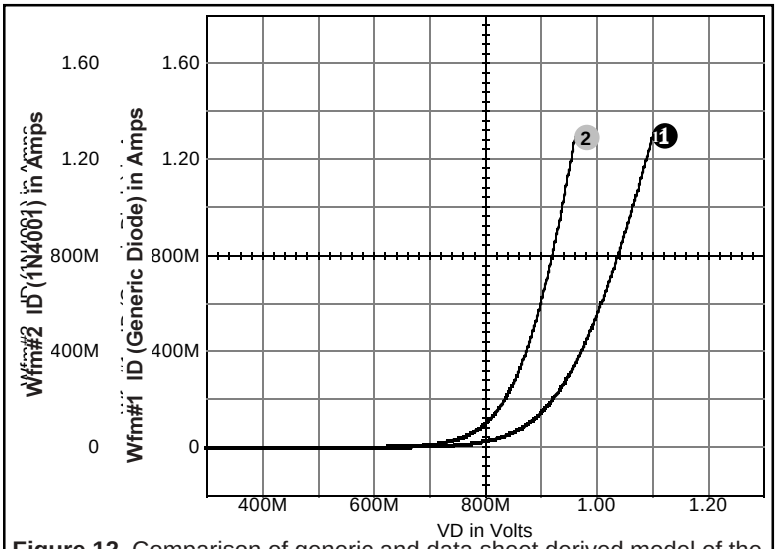


Figure 12, Comparison of generic and data sheet derived model of the 1N4001 diode.

must be reduced for the model to behave more like the real device. Parameter tweaking is not uncommon when modeling any device; in fact, it's encouraged.

Modeling Schottky Barrier or Germanium Diodes

For Schottky barrier diodes, EG, the energy gap should be .69. For germanium diodes, EG should be .67. For Schottky barrier diodes, XTI, the saturation current temperature exponent, should be 2.0. The emission coefficient is closer to 2.0 for Schottky barrier diodes, in contrast with the average PN diode which is closer to 1.0. Additionally, the saturation current, IS, will be one to two orders of magnitude higher than IS in the junction diode. The rest of the diode parameters are calculated as before.

Generic Zener Diodes

A simple zener diode can be simulated by making the breakdown voltage parameter, BV, equal to the Zener voltage, VZ, and making the current at breakdown, IBV, equal to the Zener current, IZT. However, this approximation leaves out some other important parameters. By using the enhanced generic zener model, all relevant parameters will be taken into account.

Two zener diode families have been modeled. They are in DEVICE.LIB and DEVICE2.LIB, and are modeled as subcircuits called LZEN and HZEN in order to distinguish between the low and high voltage families. The only parameter you need to enter is the breakdown voltage, BV.

Syntax: XNAME 1 2 LZEN {ZV=#}
Example: XD1 8 3 LZEN {ZV=9.1}

LZEN models the 1N746-759 and 1N4370-4372 family for voltages from 2.4 to 12.0 volts. HZEN models the 1N957-992 family for voltages ranging from 6.8 to 200 Volts. Zener impedance is computed using a polynomial function, and the typical values are 50% of the data sheet maximum. Temperature coefficients are not modeled. Dynamic parameters and forward conduction characteristics are estimated, however, these parameters are not given in vendor data sheets. Circuit dependence on these unspecified parameters is risky because different vendors are free to use any process to produce parts that meet only JEDEC specifications.

Zener Diode breakdown voltage and impedance are related because of the test circuit specification. The families modeled here have relatively high test currents. If a device is supplied that also has maximum impedance, your typical operating point will be substantially lower than the diode breakdown voltage. We have used the series resistance to compute the breakdown voltage at the lower current which is used in the simulation via the following equation:

$$IBV = ITEST,\ BV = ZV - ITEST * RS \qquad \text{Eq. 1.19}$$

where RS is a polynomial function of ZV, and ITEST is 20mA for LZEN and .125/ZV for HZEN.

Note that the polynomial function in DEVICE.LIB is scaled by .5 to account for the nominal versus maximum specification. Changing this scaling constant for both the breakdown and series resistance equations in DEVICE.LIB will show how "worst case" devices change your circuit behavior.

Junction capacitance can be calculated as a function of breakdown voltage, based on Sze [7-1, chapter 2, eq. 18, 22, 79]. For abrupt junctions, CJO = KA(VB) $^{-.665}$ and linear junctions give CJO=KL(VB) $^{-.825}$. The information given in Sze [7-1, figure 26 and 28] leads to the conclusion that high voltage zeners are more likely to use abrupt junctions (M=.5) and low voltage devices would use linearly graded junctions (M=.33), hence the choice of the capacitance exponent and grading coefficients in the two models. Both Zener diode models, LZEN and HZEN, are shown below.

```
**********
*MODEL FOR 1N746-1N759 AND 1N4370-4372 ZENERS
.SUBCKT LZEN 1 2
D1 1 2 DZEN
.MODEL DZEN D(N=1.27IBV=20MA RS={0.5*(3.8263+27.7*ZV-
+ 9.0796*ZV^2+.9678*ZV^3-.03237*ZV^4)}
+ BV={ZV-0.5*.02*(3.8263+27.7*
+ ZV-9.0796*ZV^2+.9678*ZV^3-.03237*ZV^4)}
+ CJO={1560P*ZV^-.825} TT=50N M=.33 VJ=.75 IS=1E-11)
.ENDS
**********
.SUBCKT HZEN 1 2
D1 1 2 DZEN
.MODEL DZEN D(RS= {0.5*(-2.883224E0 + 7.217979E-1*ZV
+ 5.562566E-2*ZV^2-1.139204E-3*ZV^3+1.793862E-5*
+ ZV^4-8.529727E-8*ZV^5+1.226089E-10*ZV^6)}
+ BV={ZV-0.5*.125/ZV*(-2.883224E0 + 7.217979E-1*ZV +
+ 5.562566E-2*ZV^2+ -1.139204E-3*ZV^3 + 1.793862E-
+ 5*ZV^4 -8.529727E-8*ZV^5 +1.226089E-10*ZV^6)}
+ CJO={3500P*ZV^-.665} TT=20N N=2 IS=1E-9 IBV={.125/ZV})
.ENDS
**********
```

Chapter 2 - BJTs

Bipolar Junction Transistors

Syntax: QNAME Collector Base Emitter <Substrate> Modelname
+ AREA OFF IC=VBE, VCE

Example: QPWR 1 2 3 QN3055A
.MODEL QN3055A NPN IS=4.66P BF=360 XTB=1 TR=2.55U
+TF=80N CJC=212P CJE=580P IKF=.25 PTF=120 XTF=1
+ITF=3ISE=33.4P ISC=15N RB=3 IRB=1M RBM=.4 RC=.04
+NE=1.5 MJC=.4 MJE=.4 VJC=1.8 VJE=.75 BR=2 VAF=100

The IsSpice4 BJT is based on the Gummel-Poon [2-1] integral charge control model. The IsSpice4 model actually extends the original Gummel-Poon model to include several effects at high bias levels. It reverts to the Ebers-Moll [2-2] model when certain parameters are not specified. The large and small signal models, shown schematically on the next page, are described more fully by Nagel, [2-3].

Default BJT Limitations

Like the diode, the forward and reverse storage transit time are zero (TF, TR). Charge storage (CJE, CJC) is also neglected. The forward and reverse short circuit current gains (BF, BR) do

not vary with the operating point. The ohmic resistances (RE, RB, RC) are ignored. The effect of the saturation current (IS) on VBC (early effect) is ignored. Other effects that are not modeled include large geometry effects, forward or reverse second breakdown, and thermal feedback that causes junction temperature to rise as a function of power dissipation.

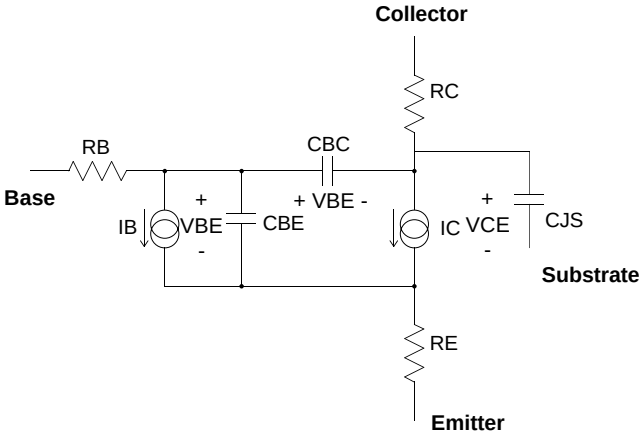


Figure 1, Large signal equivalent circuit for the charge control model of Gummel-Poon. Model shown is for NPN devices.

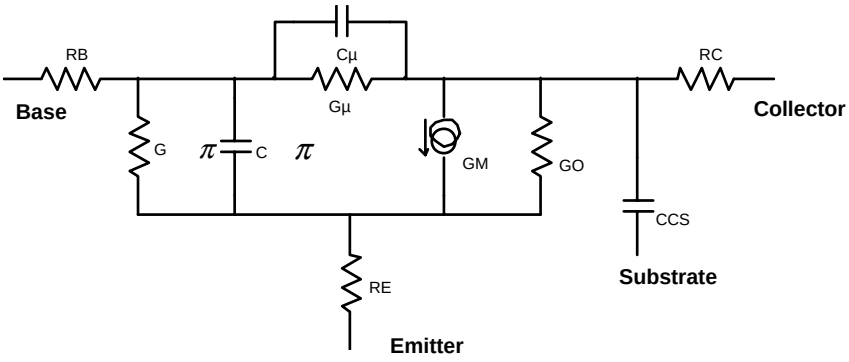


Figure 2, Small signal equivalent circuit for the charge control model of Gummel-Poon. Model shown is for NPN devices.

The IsSpice4 BJT Model

The IsSpice4 BJT large signal (Transient, Nonlinear DC analyses) and small signal (AC analysis) models are shown in Figures 1 and 2, respectively. The ohmic resistance of the collector, base and emitter regions are modeled by the linear resistors, RC, RB, RE. When these resistors are given values, nodes are added to the model, which causes longer simulation run time and reduces the available memory for the simulation. Some Intusoft IsSpice4 models for transistors only use the collector resistance in order to minimize the model's memory requirements. The two nonlinear current sources, IC and IB, determine the BJT DC characteristics.

The value of IC and IB are defined by the following equations:

$$IC = \frac{IS}{QB}\left(e^{\frac{VBE}{NF * VT}} - e^{\frac{VBC}{NR * VT}}\right) - \frac{IS}{BR}\left(e^{\frac{VBC}{NR * VT}} - 1\right) - ISC\left(e^{\frac{VBC}{NC * VT}} - 1\right) \quad \text{Eq. 2.1}$$

$$IB = \frac{IS}{BF}\left(e^{\frac{VBE}{NF * VT}} - 1\right) - ISE\left(e^{\frac{VBE}{NE * VT}} - 1\right) + \frac{IS}{BR}\left(e^{\frac{VBC}{NR * VT}} - 1\right) + ISC\left(e^{\frac{VBC}{NC * VT}} - 1\right) \quad \text{Eq. 2.2}$$

While these equations and the evaluation of their coefficients appear formidable, you should remember that most applications will reverse bias the collector-base junction, which effectively eliminates all terms involving VBC (shaded areas).

QB is approximated by the following equation:

$$QB = .5 * Q1\left(1 + \sqrt{1 + 4Q2}\right) \quad \text{Eq. 2.3}$$

where Q1 is the depletion layer stored charge and Q2 is the excess majority carrier base charge that results from injected minority carriers. Q1 and Q2 are defined in the following equations:

$$Q1 = \frac{1}{1 - \frac{VBC}{VAF} - \frac{VBE}{VAR}} \quad \text{Eq. 2.4}$$

$$Q2 = \frac{IS}{IKF}\left(e^{\frac{VBE}{NF * VT}} - 1\right) + \frac{IS}{IKR}\left(e^{\frac{VBC}{NR * VT}} - 1\right) \quad \text{Eq. 2.5}$$

If the terms ISC and ISE are zero and VAF, VAR, IKF and IKR are infinite, then the model reverts to the Ebers-Moll model, which is the ISSPICE4 default.

The terms IS,NF,ISE,NE,IKF,BF and VAF can all be evaluated with the base-emitter forward biased and the base-collector reverse biased. The reverse counterparts NR,ISC,NC,IKR,BR and VAR can be found by exchanging the collector and emitter of the transistor, or by making measurements. The latter method describes the saturation characteristics of the device, and is usually all that is available from data sheets.

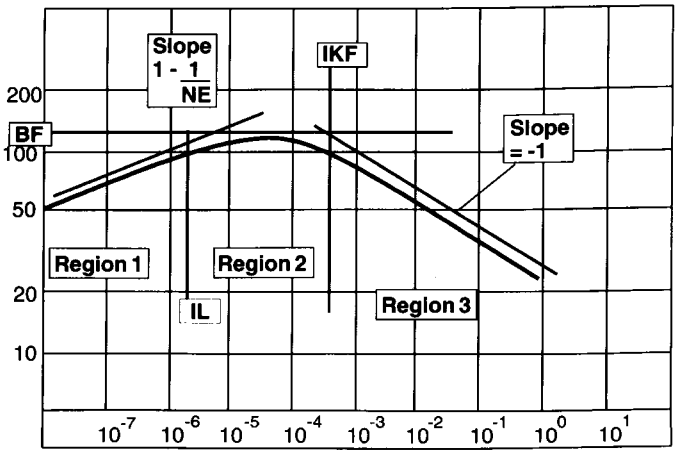


Figure 3, Current Gain as a function of collector current reveals the change in Beta with IC and how BF, IKF, NE, and ISE control the current gain behavior.

This model provides three regions of operation that are a function of collector current. Both high and low current regions will exhibit a fall-off in current gain that is controlled by IKF for high currents, and the combination of NE and ISE for low current behavior. In the mid region, behavior is determined by BF, NF and IS. All of the parameters except for VAF can be determined from plots of log(IC,IB) vs. VBE. VAF is the small

signal output resistance multiplied by the collector current in the mid region. Figure 3 shows the parameter relationships in the forward active region when the log(IC,IB) vs. VBE data is available.

Base Resistance

The base resistance, RB, can be modeled as a nonlinear function of the DC operating point using the following equations by also specifying RBM or both RBM and IRB.

If IRB is not specified:

$$RBB = RBM + \frac{RB - RBM}{QB} \qquad \text{Eq. 2.6}$$

If IRB and RBM are specified:

$$RBB = 3(RB - RBM)\frac{Tan(Z) - Z}{Z * Tan(Z)^2} \qquad \text{Eq. 2.7}$$

where:

$$Z = \frac{-1 + \sqrt{1 + \frac{144 * IB}{\pi^2 * IRB}}}{24\,\pi^2 \sqrt{\frac{IB}{IRB}}} \qquad \text{Eq. 2.8}$$

Determining DC Model Parameters from Data Sheets

Vendor data sheets usually don't provide sufficient detail to define the DC model parameters from the plot of Figure 4; however, data is generally available to calculate model parameters, based on the procedures outlined in this section. The following data is the minimum required to extract DC parameters.

HFE as a function of collector current
VBE as a function of base or collector current at or near maximum HFE and with the base-collector reverse biased

IS: Saturation Current, Default=1E-16
NF: Forward Current Emission Coefficient, Default=1
BF: Ideal Maximum Forward Bias Beta, Default=100

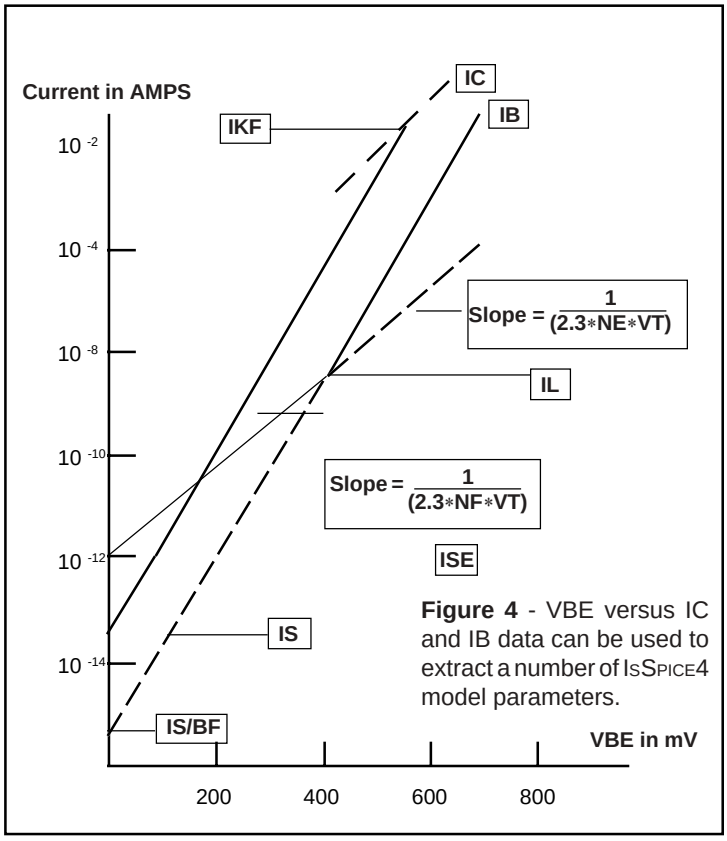


Figure 4 - VBE versus IC and IB data can be used to extract a number of ISSPICE4 model parameters.

BF is the maximum HFE value as a function of current.

IS and NF are found using the techniques used to find IS and N in the Diodes section . Be sure to multiply IS by BF if you use base current instead of collector current.

VAF: Forward Early Voltage, Default= ∞

VAF will usually range between 50 and 200 volts. If you have small signal parameters available

$$VAF = \frac{IC}{hoe(IC)}$$ otherwise, set VAF = 100

IKF: Corner for BF High Current Rolloff, Default= ∞

IKF is the collector current at which HFE is 50% below its maximum value, in the high injection region.

NE: B-E Leakage Emission Coefficient, Default=1.5
ISE: B-E Leakage Saturation Current, Default=0

The second term in equation 3.2 causes an increase in base current at low base-emitter voltage. The current at which the first 2 terms are equal is the 50% HFE fall-off on the low current side of the HFE vs IC curve. The slope is given by:

$$\frac{d(HFE)}{d(\log(IC))} = 1 - \frac{NF}{NE}$$

For integrated circuits, NE is usually near 2 and NF is near 1.

$$ISE = \frac{IC\ (50\ \%)}{\left(BF * e^{\left(\frac{VBE}{(NE * VT)} \right)} \right)}$$

RB: Zero Bias Base Resistance, Default=0
RC: Collector Resistance, Default=0
RE: Emitter Resistance, Default=0

In most applications, it is sufficient to model the ohmic collector resistance, RC. RC is used to account for the increase in saturation voltage at high current.

$$RC = \frac{(VCE - VSAT)}{IC}$$

where VCE and IC are data sheet specifications and VSAT is the value predicted by the model with RC = 0.

Many small signal applications have a relatively high value of base resistance compared to the value calculated using the curves of Figure 4. If this higher value causes incorrect large signal behavior, then it will be necessary to specify RBM, causing the base resistance to become lower at high currents.

To shape the nonlinearity further, you can specify IRB, the current at which RB falls to half its zero bias value. Beware of device models that contain large values (> 10 Ohms) for RB without the specification of IRB and RBM. Their small signal behavior may be correct, but they will be incorrectly biased.

Reverse Parameters

The reverse parameters, BR,VAR,IKR,NR and ISC will not affect operation in the forward linear region. With the exception of VAR, these parameters will cause changes in saturation voltage. RC is usually dominant for high currents, and BR can be used to establish a saturation voltage at low currents, while leaving the other parameters at their default values. Specialized applications, such as chopper switches that operate the transistor with the collector and emitter interchanged, will require that experimental data be taken.

BJT Dynamic Parameters

The nonlinear capacitances (CBE and CBC) account for charge storage in the BJT model. The following equations express the relationship of the model parameters to these capacitances:

Junction Capacitance

$$CBE = TFF \frac{IS}{QB * VT * NF} e^{\frac{VBE}{NF * VT}} + \frac{CJE}{\left(1 - \frac{VBE}{VJE}\right)^{MJE}} \quad \text{Eq. 2.9}$$

$$CBC = TR \frac{IS}{VT * NR} e^{\frac{VBC}{NR * VT}} + \frac{CJC}{\left(1 - \frac{VBC}{VJC}\right)^{MJC}} \quad \text{Eq. 2.10}$$

$$CSS = \frac{CJC}{\left(1 - \frac{VCS}{VJS}\right)^{MJS}} \quad \text{Eq. 2.11}$$

where:

$$TFF = TF\left(1 + VTF\left(\frac{IF^{2}}{(IF + ITF)^{2}} e^{\frac{VBC}{(1.44 * VT)}}\right)\right)$$ Eq. 2.12

$$IF = IS\left(e^{\frac{VBE}{NF*VT}} - 1\right)$$ Eq. 2.13

Forward Biased Capacitance:

All capacitances of the form: $\frac{CO}{\left(1-\frac{V}{\Phi}\right)^{M}}$ Eq. 2.14

revert to the form:

$$\frac{CO}{(1-FC)^{1+M}}\left\{1-FC(1+M)+M\frac{V}{\Phi}\right\}$$ Eq. 2.15

when V > FC, and FC taken as 0 for CSS.

Determining Dynamic Parameters from Data Sheets

The first terms of equations 3.9 and 3.10 describe stored charge from minority carrier injection, and the second terms represent voltage dependent depletion layer capacitance. You can refer to the Diodes section for determining the ISSPICE4 parameters for depletion layer capacitance.

TF: Forward Transit Time, Default=0

The forward transit time determines the transistor gain bandwidth product in the forward active region. The transistor gain bandwidth product in the forward active region is:

$$\frac{1}{2\pi F_t} = TF * QB + \frac{VT}{IC}\left(\frac{CJE}{\left(1-\frac{VBE}{VJE}\right)^{MJE}} + \frac{CJC}{\left(1-\frac{VBC}{VJC}\right)^{MJC}}\right)$$ Eq. 2.16

Maximum Ft occurs when operating at collector current below

IKF and for high VCB. Under these conditions, the above equation simplifies to:

$$TF = \frac{1}{2\pi F_t} \qquad \text{Eq. 2.17}$$

Maximum Ft is usually found in the data sheet.

TR: Reverse Transit Time, Default=0

Reverse transit time (TR) is primarily responsible for transistor storage time and is determined from pulsed turn-off tests, [3-4].

$$TR = \frac{\frac{Ts}{BR}}{\ln\left(\frac{IB1 + IB2}{\frac{IC1}{IF} + IB2}\right)} \qquad \text{Eq. 2.18}$$

where:

Ts	is the storage time
IC1	is the initial collector current when the transistor is saturated
IB1	is the forward base current used to turn the transistor on.
IB2	is the reverse base current used to turn the transistor off.

For the ISSPICE4 default of BR = 1, BF = 100 and for the typical test condition of IB1 = IB2, the equation simplifies to:

$$TR = 0.6 * Ts$$

BJT AC Parameters

Several additional parameters are used for the ISSPICE4 AC analysis to model transistor noise. The resistors RC, RB and RE are each given an equivalent noise current of:

Bulk resistor Noise:

$$I^2 = 4 * K * T * \frac{B}{R} \qquad \text{Eq. 2.19}$$

where I is the spectral noise, Amps/RTHz
K is Boltzman's constant, 1.38E-23 Joules/Kelvin
T is temperature in Deg. Kelvin
B is Bandwidth in Hz

The AC analysis will sum the square of the noise currents, and assume a noise bandwidth, B, of 1 Hz. Shot and flicker noise are modeled for the base and collector currents by:

Shot and Flicker Noise:

$$\ln^2 = 2*q*I*B + KF*B*(I)\frac{AF}{F} \qquad \text{Eq. 2.20}$$

where In is the spectral noise, $Amps\ \sqrt{Hz}$. F is the analysis frequency, q is the charge of an electron, 1.6E-19 Coulombs.

AF and KF can be estimated from data sheets when information is available, otherwise assume the two terms are equal at about 1KHz, and solve for KF with AF=1, the default value. This estimate yields KF = 3.2E-16.

In the AC analysis, phase is a linear function of frequency, with PTF specifying the phase, in degrees, at Ft.

BJT Temperature Parameters

$$\frac{IS\ (T\ )}{IS\ (T_{NOM}\ )} = \left(\frac{T}{T_{NOM}}\right)\frac{XTI}{NF}\exp\left[\left(\frac{EG}{NF*VT}\right)\left(\frac{T\ -\ T_{NOM}}{T_{NOM}}\right)\right] \qquad \text{Eq 2.21}$$

For ISE and ISC, NF =1.

$$\frac{ISE(T)}{ISE(T_{NOM})} = \left(\frac{T}{T_{NOM}}\right)\frac{XTI}{NE} - XTB\exp\left[\left(\frac{EG}{NE*VT}\right)\left(\frac{T-T_{NOM}}{T_{NOM}}\right)\right] \qquad \text{Eq 2.22}$$

$$\frac{ISC(T)}{ISC(T_{NOM})} = \left(\frac{T}{T_{NOM}}\right)\frac{XTI}{NC} - XTB\exp\left[\left(\frac{EG}{NC*VT}\right)\left(\frac{T-T_{NOM}}{T_{NOM}}\right)\right] \qquad \text{Eq 2.23}$$

$$BF\ (T\ ) = BF\ *\left(\frac{T}{T_{NOM}}\right)^{XTB} \qquad \text{Eq 2.24}$$

$$BR(T) = BR*\left(\frac{T}{T_{NOM}}\right)^{XTB} \qquad \text{Eq 2.25}$$

For both the Collector (VJC) and Emmiter (VJE) junctions;

$$VJ\ (T\ ) = VJ\ *\left(\frac{T}{T_{NOM}}\right) - 2*VT\ *\ln\left(\frac{T}{T_{NOM}}\right)^{1.5} - \left[\left(\frac{T}{T_{NOM}}\right)*EG\ (T_{NOM}\ ) - EG\ (T\ )\right] \qquad \text{Eq 2.26,2.27}$$

An Enhanced BJT Default

The BJT default in IsSPICE4 gives first order, Ebers-Moll, DC parameters; but it does not provide parameters for Transient or AC analysis. The following default can be used when minimal data sheet specifications are available by using the PARAM program to evaluate the equations in curly braces. This model will create a good transistor model from virtually any data sheet. The parameters you must specify are:

IMAX	Maximum collector current
COB	Collector-base capacitance
FT	Gain bandwidth product in Hz
TS	Storage time

The equation-based model is shown below:

```
.MODEL NBJT NPN (CJC={2.2*COB} TF={.16/FT} TR={1.7*TS}
+CJE={7*COB} RC={.5/IMAX} VAF=100 IKF={.7*IMAX}
+ IS={2E-15*MAX} )
```

This subcircuit-based macro model makes use of the default model parameters so that it is not permissible to change default values without reevaluating the parameters which are given here.

Model Limitations

The IsSPICE4 BJT model limitations include the limitations listed for diodes as well as:

Neither forward nor reverse bias second breakdown is modeled.

Large geometry effects are not modeled.

Power Transistors

The turn-off behavior of the power BJT can be approximated by paralleling BJTs and using a base resistor to connect the bases of the transistors. The topology shown in the subcircuit below will produce the turn-off tail associated with quasi-saturation. The value of RB and IKF will tend to control the turn-off tail.

```
.SUBCKT NPWR 1 2 3
Q1 1 2 3 QPWR AREA=.67
Q2 1 4 3 QPWR AREA=.33
RB 2 4 {RB}
.MODEL NPWR NPN(...IKF=...)
.ENDS
```

The generic power transistor subcircuit, "NPWR" can be found in DEVICE.LIB.

For medium power BJTs (40-200V, 5-50 Amps) the standard Gummel-Poon model may be used. Modeling more complex effects such as the nonlinear variation of collector resistance with current will require the use of nonlinear resistors in the collector and base regions.

References

[2-1] AN INTEGRAL CHARGE CONTROL MODEL OF BIPOLAR TRANSISTORS
H.K. Gummel and H.C. Poon, Bell System Technical Journal, Vol 48, May-June, 1970 pp 827-852.

[2-2] LARGE SIGNAL BEHAVIOR OF JUNCTION TRANSISTORS
J.J. Ebers and J.L. Moll, Proc. IRE, Vol. 46, Nov. 1952.

REFERENCES

[2-3] SPICE2: A COMPUTER PROGRAM TO SIMULATE SEMICONDUCTOR CIRCUITS
L.W. Nagel, Memorandum No. ERL-M520, May 1975, Electronics Research Laboratory, College of Engineering, University of California, Berkeley

[2-4] PARAMETER DETERMINATION TECHNIQUES FOR THE GUMMEL-POON CAD TRANSISTOR MODEL
J.C.Bowers, N. English and H.A.Nienhaus, Power Electronics Specialists Conference Proceedings pp 83-90, June 1980

Chapter 3 - JFETs

Junction Field Effect Transistors

Syntax: JNAME Drain Gate Source Modname
+<Area> <Off> <IC=Vds, Vgs>
Example: JRES 1 2 3 JFET
.MODEL JFET NJF (VTO=-1.1 BETA= 15M LAMBDA=.001
+RS=.5 RD=1.5 CGS=50P CGD=50P PB=.2 IS=1E-15)

Overview

The JFET is a device that allows a current to flow which is proportional to an electric field, basically emulating a voltage controlled resistor. It has a variety of applications in analog switching, high input impedance amplifiers and various integrated circuits. The IsSpice4 JFET model is taken from the quadratic FET model of Shichman and Hodges, [3-1]. The large and small signal IsSpice4 models for an n-channel JFET are shown in Figure 1. The p-channel model is schematically identical, except that all polarities are reversed. RD and RS are linear resistors that model the ohmic resistance of the drain and source. The pn junctions between the gate and source and gate and drain terminals are modeled by the two parasitic diodes. Charge storage is modeled by two nonlinear depletion layer capacitors, CGS and CGD, and model parameter PB.

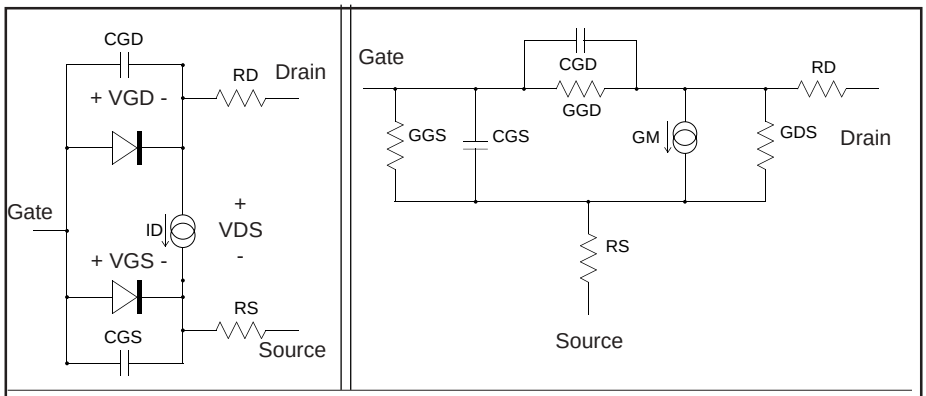


Figure 1, Large signal model, left, has diodes modeled similar to the standard diode, Except N = 1 and PB replaces VJ. Small signal model shown to the right. Models shown are for N channel devices.

DC Characteristics

The DC characteristics which are determined by VTO, BETA, LAMBDA, and IS, are shown below and are modeled as follows:

Forward Region, VDS > 0 Eq. 3.1

$VG - VTO < 0$: $ID = 0$

$0 < VG - VTO < VDS$: $ID = BETA * (VGS - VTO)^2 * (1 + LAMBDA * VDS)$

$0 < -VDS < VGS - VTO$: $ID = BETA * VDS * (2 * (VGS - VTO) - VDS) * (1 + LAMBDA * VDS)$

Reverse Region, VDS < 0 Eq. 3.2

$VG - VTO < 0$: $ID = 0$

$0 < VGS - VTO < -VDS$: $ID = BETA * (VGS - VTO)^2 * (1 - LAMBDA * VDS)$

$0 < -VDS < VGS - VTO$: $ID = BETA * VDS * (2 * (VGS - VTO) - VDS) * (1 - LAMBDA * VDS)$

When dealing with FETs, the region of linear circuit operation is known as the forward saturated region, (VGS - VTO) < VDS, and the linear region is named for the linear relation between drain current and gate voltage when VDS < (VGS - VTO). This reversal of names between the physical and circuit behavior may lead to confusion when circuit designers deal with the physics of semiconductor devices. N-channel JFETs usually

have a negative threshold, and by convention the p-channel JFET threshold is also negative for IsSpice4. Positive values of VTO are used when enhancement mode behavior is required.

The diodes in the JFET are described in the same manner as in equation 4.1 except that the emission coefficient, N, is taken as 1; it cannot be varied in the JFET model. The PN junctions between the gate and the channel of a real JFET are subject to breakdown, however, this effect is not modeled in IsSpice4.

Dynamic Behavior

JFET dynamic parameters are determined by the nonlinear capacitors, CGS and CGD. The capacitance values are computed using the same equations as for diodes with PB replacing the term VJ. The junction grading coefficient (M) is set to .5 and cannot be varied in the IsSpice4 JFET.

Noise

Thermal, shot, and flicker noise are modeled in the JFET.

Resistor Noise (RS and RD):

$$I^2 = 4 * k * T * \frac{B}{RS}$$ Eq. 3.3

$$I^2 = 4 * k * T * \frac{B}{RD}$$ Eq. 3.4

Shot and Flicker Noise:

$$ID^2 = 8 * K * T * \frac{gm}{3} + KF * ID\frac{AF}{f}$$ Eq. 3.5

where gm is the small signal transconductance of the JFET, k is Boltzman's constant and T is temperature in degrees Kelvin.

Temperature Dependence

IsSpice4 accounts for the temperature dependence of the parameters related to the parasitic diodes, IS, FC, PB, CGS, and CGD. The IsSpice4 TEMP options parameter is used to vary the simulation temperature.

Determining JFET Parameters from Data Sheets

VTO: Threshold Voltage, Default = -2

The threshold voltage is usually given explicitly. Sometimes a closely related parameter, the gate-source cutoff voltage, VGS(off), is specified. The threshold is usually somewhat greater than the cutoff voltage; however, it is close enough for most applications. VTO is negative for both N and P channel depletion JFETs. VTO is positive for enhancement mode JFETs (See Figure 2).

BETA: Transconductance, Default = 1E-4

BETA is related to transconductance in the forward saturated region by:

$$gm = 2 * BETA * (VGS - VTO) \qquad \text{Eq. 3.6}$$

or equivalently by:

$$BETA = \frac{IDSS}{VTO^2} \quad \text{when } VGS = 0 \qquad \text{Eq. 3.7}$$

In the forward linear region, the ON conductance is:

$$gon = 2 * BETA * (CGS - VTO) \quad \text{when VDS=0} \qquad \text{Eq. 3.8}$$

Data sheet specifications will usually allow one of the above forms to be used to obtain BETA. JFETs used as amplifiers will usual specify tranconductance and equation 4.6 will give BETA. Switching devices will specify IDSS and power devices Gon or Ron, making equation 4.7 or 4.8 appropriate (See Figure 3).

LAMBDA: Channel Length Modulation Parameter, Default = 0

The output conductance, Gds, is related to LAMBDA in the forward saturated region as follows:

$$gds = BETA * LAMBDA * (VGS - VTO)^2 = LAMBDA * ID \quad \text{Eq. 3.9}$$

Amplifier data sheets will usually specify the small signal output conductance and will either give ID or specify that VGS = 0. LAMBDA's value is typically between 0.1 and 0.01 V^{-1}. This parameter plays the same role as VAF for BJTs, except its units are reciprocal volts. LAMBDA = .02 is a good default if insufficient information is given (See Figure 4).

RS and RD: Source and Drain Ohmic Resistances, Default=0

The resistance RS should be included in the model to account for the variation in output conductance in the saturation region. Normally, as VGS is decreased in value, the value of current will rise exponentially. RS is the slope of the ID vs VGS curve in the saturation region. To change the rate at which the current rises with decreasing VGS, increase the value of RS.

The resistance RD is used to vary the response in the linear region. Without RD, the linear region characteristic curves will tend to be overly steep. Adding RD will decrease the slope of the linear region characteristic as shown in Figure 5.

CGS and CGD: Nonlinear Junction Capacitors, Default = 0
PB: Gate Junction Potential, Default = 1
M: Junction Grading Coefficient, Set at .5

CGS and CGD are voltage dependent depletion region capacitors having the same response as that of the diode capacitance, CJO. Calculation of CGS and CGD should proceed in the same manner as for the diode capacitance. If reverse voltage data is not available, however, commonly supplied values for Ciss (input capacitance) and Crss (reverse transfer capacitance) may be used.

$$CGS = Ciss - Crss \quad \text{Eq. 3.10}$$
$$CGD = Crss \quad \text{Eq. 3.11}$$

The value of M is set to .5 and cannot be changed. PB is equivalent to the diode VJ parameter, and is found using similar methods (Eq. 1.15) Other parameters can be determined in the same manner as described for diodes.

Parameter Tweaking

The graphs on the following page can be used as a guide when creating a JFET model. The graphs will give you an idea of how to vary or tweak important parameters in order to achieve the correct device response.

The following test circuit may be used to generate a set of DC characteristic curves. The accuracy of the parameter set can then be determined, and any appropriate variables may be tweaked to refine the model.

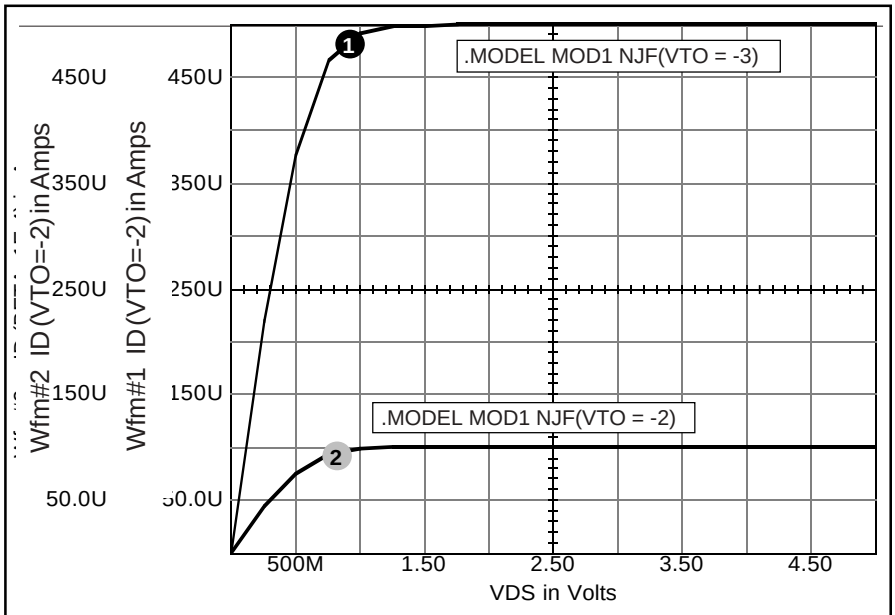


Figure 2, ID vs. VDS for various values of Threshold, VTO.

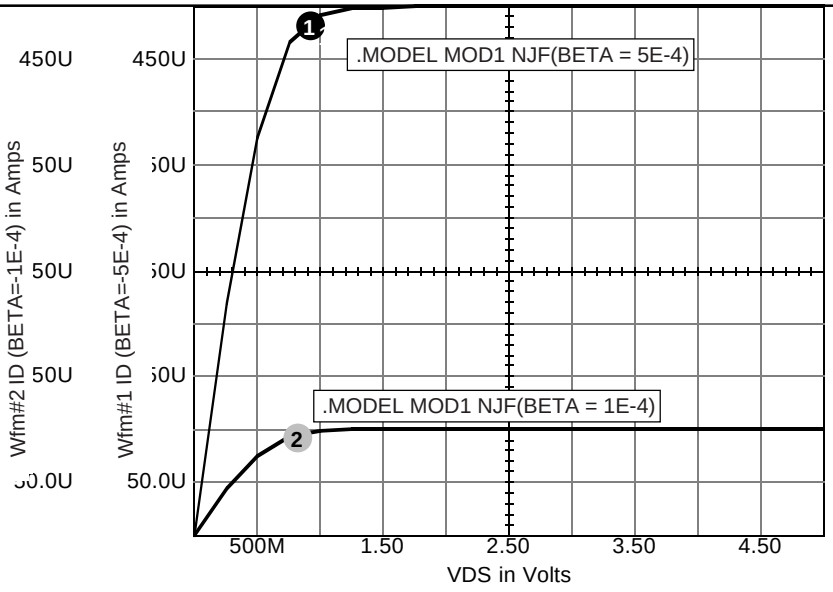


Figure 3 , ID vs. VDS for various values of BETA.

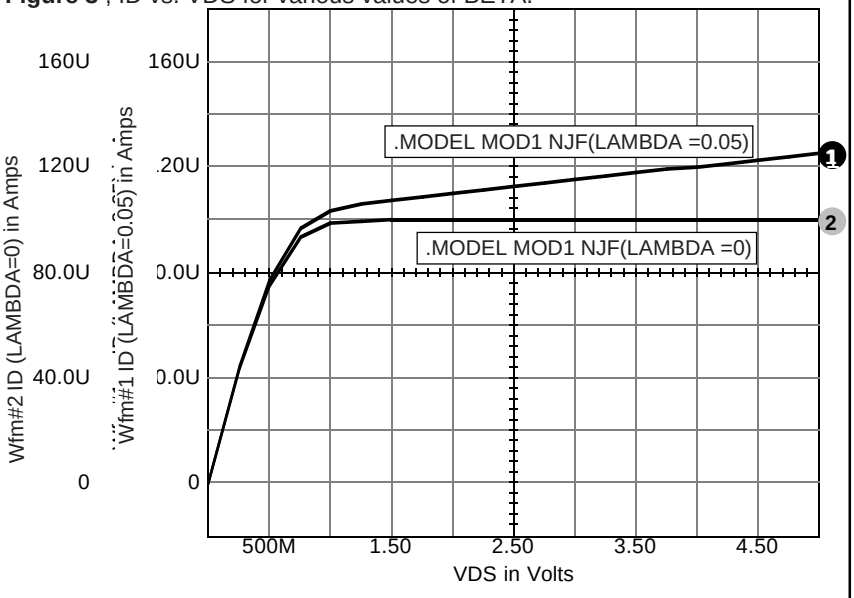
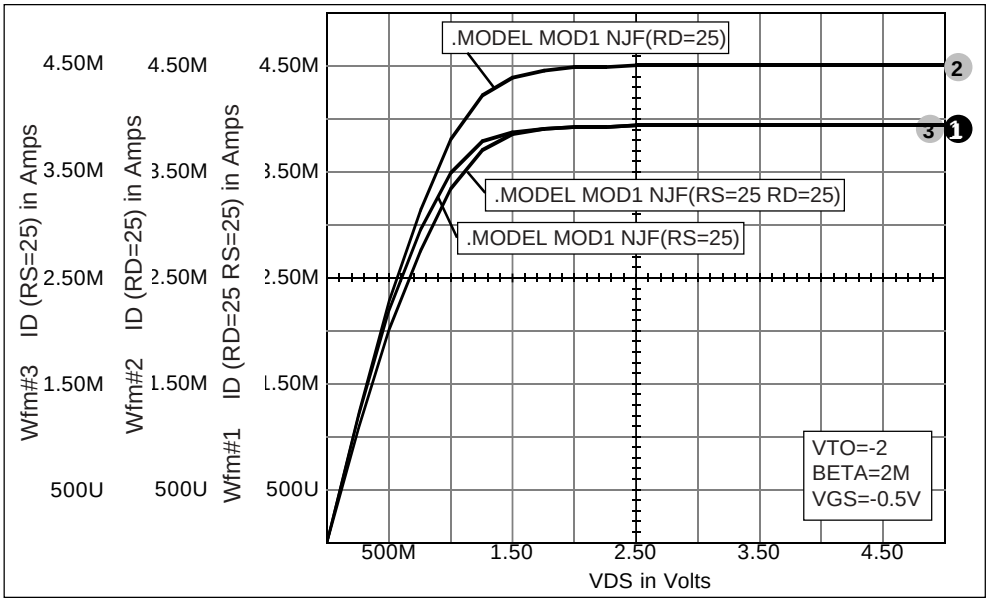


Figure 4, ID vs. VDS for various values of the channel length modulation parameter, Lambda.




```
JFET CHARACTERISTICS
.DC VDS 0 5 .25
.MODEL MOD1 NJF
*VIDS measures ID. Could have
*used VDS, but ID would
*be negative
.PRINT DC  I(VIDS)
VIDS  1  2
VDS  1  0
J1  2  7  0  MOD1
VGS  7  0 -1
.END
```

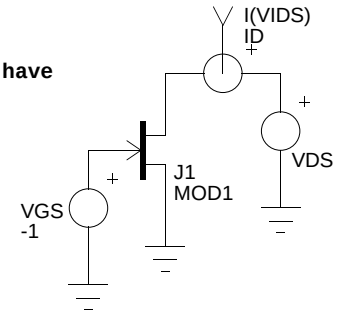


Figure 6, The simple circuit shown above can be used to generate a characteristic set of curves. The line ".MODEL MOD1 NJF ..." should contain the model under investigation.

Gallium Arsenide FET: (GaAsFET)

In addition to the built-in GaAsFET model in IsSPICE4, a GaAsFet subcircuit can be built using an equivalent circuit with either a JFET or a MOSFET. Like the MOSFET, the GaAsFET has the "rear" electrode replaced by a substrate. Unlike the MOSFET, the substrate is nearly a perfect insulator. The gate contact is either a junction diode, or in the case of the MESFET, a Schottky barrier diode. The JFET is most commonly used as the starting point for GaAsFET models. The gate diodes are removed by making IS very small, and then discrete diodes are added so that the emission coefficient can be controlled. The threshold modulation in the GaAsFET which is caused by backgating through the stray capacitance causes the gain of amplifier circuits to be much higher at DC than even at a few KHz. Most GaAsFET applications are for either microwave amplifiers or high speed current mode logic, and require the DC bias effects to be modeled. The model shown in Figure 7 will take this effect into account for linear circuits, but does not give good predictions for "saturated" switching circuits. GaAsFET technology is new, so you will have to determine model parameters experimentally rather than from data sheets.

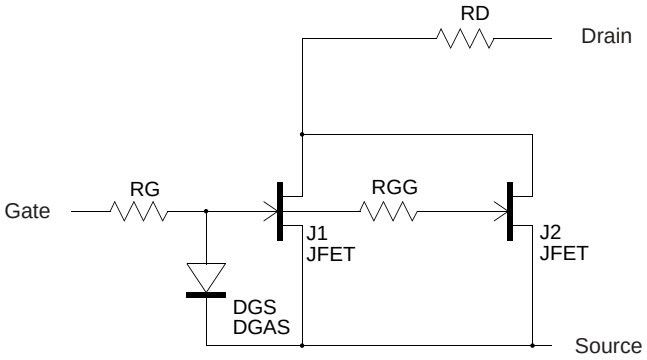


Figure 7, A GaAsFET Equivalent Circuit

Listed below is the GaAsFET subcircuit model and test circuit. The GaAsFET model requires the parameters, L, W, KP, RHOG, RHOD, DC, VT and N to be passed to the subcircuit.

```
********** GASFET MODEL AND TEST CIRCUIT **************
*       PARAMS ARE L=CHANNEL LENGTH IN MICRONS
*           W=CHANNEL WIDTH IN MICRONS
*           KP=KPRIME, ID=KP*W/L(VG-VT)^2
*           RHOG=GATE METAL OHMS/MICRON
*           RHOD=DRAIN METAL OHMS/MICRON
*           DC=CAPACITANCE/MICRON
*           VT=THRESHOLD
*           N=NUMBER OF DEVICES DEFINED BY W AND L THAT ARE IN PARALLEL
* YOU WILL PROBABLY WANT TO BUILD SOME OF THESE INTO THE MODEL
* SO THAT THEY DON'T HAVE TO BE IN THE PARAMETER LIST ALL OF THE TIME
* SUBSTRATE CAPACITIVE COUPLING IS IGNORED.
.SUBCKT GAS 1 2 3
RG 2 4 {W*RHOG/N}
RD 1 5 {W*RHOD/N}
DGS 4 3 DGAS
* THE GATE DRAIN DIODE IS NOT MODELED SINCE IT IS ALWAYS REVERSE BIASED
* THIS IS AN ESTIMATE OF A GAS JFET, SET N=1 FOR A MESFET
* FOR MORE DETAIL, SEE THE CHAPTER ON DIODE MODELS
.MODEL DGAS D(N=2)
RGG 4 6 1E10
J1 5 4 3 JFET
J2 5 6 3 JFET AREA=.33
* THE ABOVE AREA PARAMETER MUST BE DETERMINED EXPERIMENTALLY
* TO MATCH THE DEVICE SATURATION SLOPES AT HIGH FREQUENCY
.MODEL JFET NJF(BETA={KP*W/L*N} LAMBDA=.15 IS=1E-30 CGS={DC*W*N}
+  CGD={DC*W*N} VTO={VT} )
.ENDS
**************************
GASFET TEST CIRCUIT WITH EXAMPLE GASFET CALL.
.PRINT AC V(2) VP(2)
.AC DEC 10 10 100MEG
VIN 1 0 .4 AC 1
X1 2 1 0 GAS {VT=.3 KP=90U N=8 W=40 L=1 RHOD=.3 RHOG=1 DC=.25F }
RD 2 3 10K
VCC 3 0 3
*INCLUDE DEVICE.LIB
.END
```

References

[3-1] MODELING AND SIMULATION OF INSULATED GATE FIELD EFFECT TRANSISTOR SWITCHING CIRCUITS
H. Shichman and D. A. Hodges, IEEE J. Solid State Circuits, vol. SC-3, 1968

Chapter 4 - MESFETs

Metal Semiconductor Field Effect Transistors

IsSpice4 Semiconductor Primitive: **MESFET**
Call Letter: **Z**
Device Type: **N (NMF) or P (PMF) Channel**

Syntax: ZNAME Drain Gate Source Modname
+<Area> <Off> <IC=Vds, Vgs>
Example: ZRES 1 2 3 MESFET
.MODEL MESFET NMF ()

Overview

The GaAs MESFET is a Schottky-barrier gate device. Its basic operation is like the JFET. The IsSpice4 GaAs MESFET model is based on the research efforts of H. Statz, [4-1]. The large and small signal equivalent circuits for an n-channel MESFET is shown in Figure 1. The p-channel model is schematically identical except that all polarities are reversed.

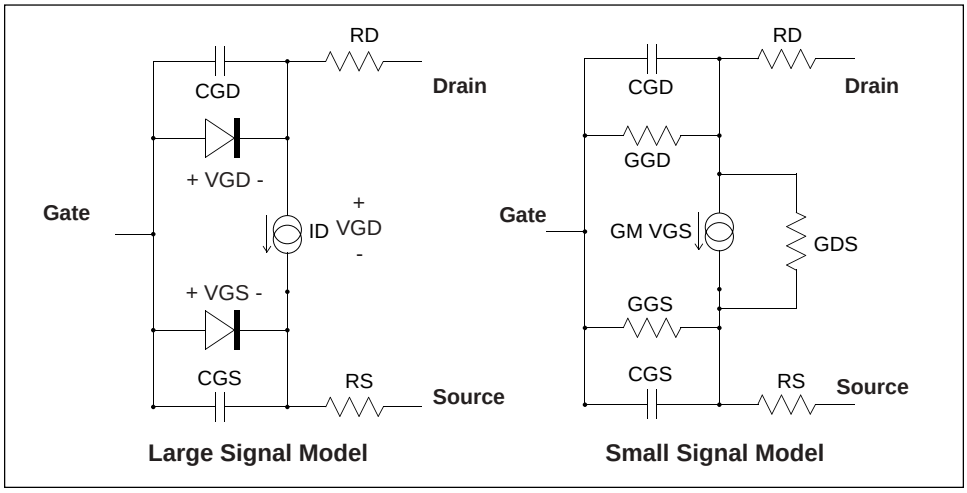


Figure 1, Large and Small signal models for the Statz *et al.* GaAs MESFET

DC Characteristics

The DC characteristics are governed by VTO, B, BETA (β), ALPHA (α), LAMBDA (λ), IS, RS, and RD as described by the following equations:

$$0 > Vds > \frac{3}{\alpha}$$

Forward Region,

$$I_d = \frac{\beta(Vgs - V_{TO})^2}{1 + b(Vgs - V_{TO})}\left[1 - \left[1 - \alpha\frac{Vds}{3}\right]^3\right](1 + \lambda Vds)$$

$$g_m = \left[1 - \left(1 - \frac{\alpha V_{ds}}{3}\right)^3\right](1 + \lambda V_{ds})\left[\frac{2\beta(V_{gs} - V_{TO})}{1 - b(V_{gs} - V_{TO})}\right] - \frac{b\beta(V_{gs} - V_{TO})^2}{[1 + b(V_{gs} - V_{TO})]^2}$$

$$g_{ds} = \left[1 - \left(1 - \frac{\alpha V_{ds}}{3}\right)^3\right]\lambda + \alpha(1 + \lambda V_{ds})\left(1 - \frac{\alpha V_{ds}}{3}\right)^2 * \frac{\beta(V_{gs} - V_{TO})^2}{1 + b(V_{gs} - V_{TO})}$$

Reverse Region, $Vds \geq \frac{3}{\alpha}$

$$I_d = \frac{\beta (V_{gs} - V_{TO})^2}{1 + b(V_{gs} - V_{TO})}(1 + V\lambda_{ds})$$

$$g_m = \frac{\left[1+b(V_{gs}-V_{TO})\right]2\beta(V_{gs}-V_{TO}) - b\beta(V_{gs}-V_{TO})^2}{\left[1+b(V_{gs}-V_{TO})^2\right]}(1+\lambda V_{ds})$$

$$g_{ds} = \frac{\lambda\beta(V_{gs}-V_{TO})^2}{1+b(V_{gs}-V_{TO})}$$

Charge Storage

The charge storage effects are modeled by CGS, CGD, and PB, along with the constants δ and V_{max} and the DC parameter ALPHA (a) by the following equations:

$$C_{GS} = \frac{CGS}{\sqrt{1-\frac{V_n}{PB}}} * \frac{1}{2} * \left[1 + \frac{V_e - V_{TO}}{\sqrt{(V_e - V_{TO})^2 + \delta^2}}\right] * \frac{1}{2} * \left[1 + \frac{V_{GS} - V_{GD}}{\sqrt{(V_{GS} - V_{GD})^2 + \left(\frac{1}{\alpha}\right)^2}}\right] + CGD * \frac{1}{2} * \left[1 - \frac{V_{GS} - V_{GD}}{\sqrt{(V_{GS} - V_{GD})^2 + \left(\frac{1}{\alpha}\right)^2}}\right]$$

$$C_{GS} = \frac{CGS}{\sqrt{1-\frac{V_n}{PB}}} * \frac{1}{2} * \left[1 + \frac{V_e - V_{TO}}{\sqrt{(V_e - V_{TO})^2 + \delta^2}}\right] * \frac{1}{2} * \left[1 + \frac{V_{GS} - V_{GD}}{\sqrt{(V_{GS} - V_{GD})^2 + \left(\frac{1}{\alpha}\right)^2}}\right] + CGD * \frac{1}{2} * \left[1 + \frac{V_{GS} - V_{GD}}{\sqrt{(V_{GS} - V_{GD})^2 + \left(\frac{1}{\alpha}\right)^2}}\right]$$

$$V_e = \frac{1}{2}\left[V_{GS} + V_{GD} + \sqrt{(V_{GS} - V_{GD})^2 + \left(\frac{1}{\alpha}\right)^2}\right]$$

$$V_n = \frac{1}{2}\left[V_e + V_{TO} + \sqrt{(V_e - V_{TO})^2 + \delta^2}\right] \quad \text{for } V_n \leq V_{max}$$

$$V_n = V_{max} \quad \text{for } V_n > V_{max}$$

Noise

The noise model for the MESFET can be taken directly from the JFET model. The model parameters AF, flicker noise exponent, and KF, flicker noise coefficient, define the noise characteristics of the MESFET.

References

[4-1] Hermann Statz, Paul Newman, Irl W. Smith, Robert A Pucel, Hermann Haus, “GaAs FET Device and Circuit Simulation in SPICE”, IEEE Trans. Electron Devices, Vol. ED-34, 1987, pp. 160-169

[4-2] Giuseppe Massobrio, Paolo Antognetti, Semiconductor Device Modeling With SPICE, Second Edition, McGraw-Hill Inc., 1993

[4-3] J. Michael Golio, Microwave MESFETs & HEMTs, Artech House, 1993

Chapter 5 - MOSFETs

Metal Oxide Semiconductor FETs

IsSpice4 Semiconductor Primitive: **MOSFET**

Syntax: MNAME Drain Gate Source Substrate L= W= AD=
+ AS= PD= PS= NRD= NRS= OFF
+ IC=VDS, VGS,VBS

Example: M1 10 7 0 0 MOD1 L=4U W=6U AD=10P AS=10P
.MODEL MOD1 NMOS VTO=-2 NSUB=1E15 UO=500
+ LEVEL=2

Overview

The MOSFET equivalent circuit is shown in Figures 1 and 2. It is similar to the JFET model, except that one of the gate electrodes has been replaced by a semiconductor substrate and the gate itself is insulated rather than made by using a P-N junction. The IsSpice4 MOSFET models are applicable to any insulated-gate FET. The MOSFET model is the only semiconductor device that has several command line options. The options are for the L (length in meters, default=100U), W (width in meters, default =100U), AD/AS (drain/source area in square meters, default=0), PD/PS (drain/source perimeter in meters, default 0), and NRD/NRS (equivalent number of squares of drain/source diffusion, default=1). The number of squares is multiplied by the model parameter RSH to find the drain and

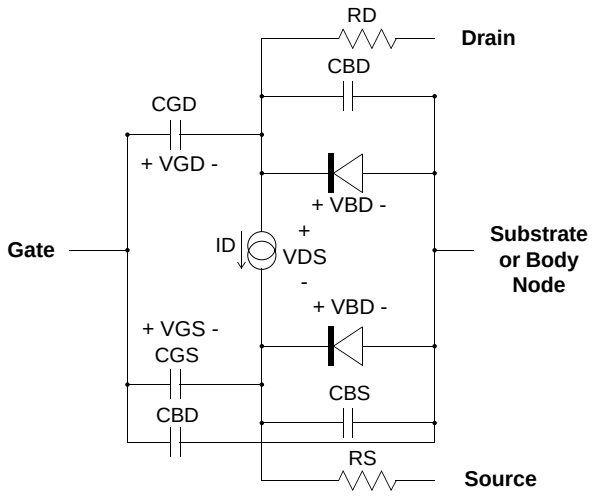


Figure 1, The IsSpice4 large signal MOSFET model is shown for an N channel device. For a P channel device V_{GS}, V_{GD}, V_{DS}, V_{BS}, V_{BD}, the two substrate junctions and the nonlinear current source I_D are reversed.

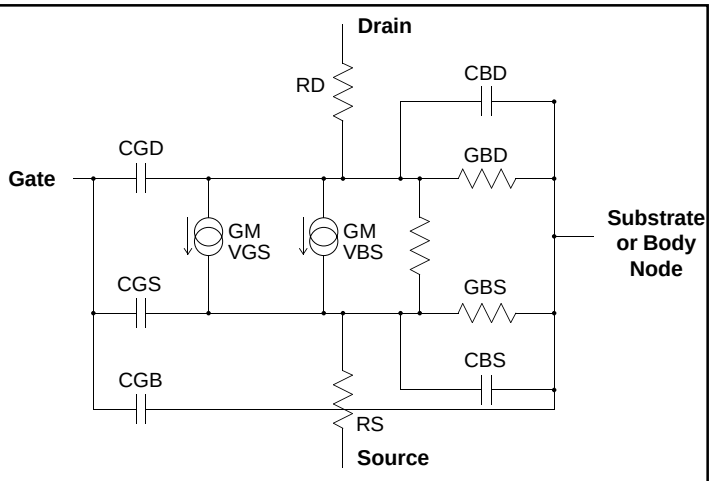


Figure 2 , The IsSpice4 small signal MOSFET model is shown for an NMOS device.

source resistances. Parameters which are not specified are left at their default values. The default value can be changed using the .OPTIONS command. Changing the defaults can simplify the input netlist, as well as the editing process. The command line parameters are very important and can dramatically effect device behavior, especially if they are specified incorrectly. If circuit behavior is erratic, the MOSFET call line is one of the first places to check.

Important Note: Be very careful when specifying the MOSFET command line parameters. The correct UNITS are essential to proper operation. L, W, PS, and PD are expressed in meters, while AD and AS are in square meters. Therefore, L, W, PS, and PD will usually have the units of "U", microns, while AD and AS will have the units of P (square-microns).

MOSFETs are fairly simple devices to build, but extremely complex devices to model. This contrasts bipolar transistors which are difficult to build, but can be modeled quite accurately in spite of the various topologies and material compositions used in bipolar technology. Because of various modeling limitations, no one model can be used for all MOSFETs. A number of models are now in use, each with its own set of restrictions and features.

Modeling a MOSFET is quite complicated. Each level has a different set of parameters and procedures for calculating IsSPICE4 parameter values. The required depth and breath of the resulting discussion is beyond the scope of this text. A designer using integrated MOSFETs can usually obtain the device models from the manufacturer. An exception to this rule concerns power MOSFETs which are explained in the SPICEMOD (SPICE modeling program) User's Guide. If you plan to model or characterize MOSFET devices, however, you should become intimately familiar with references [5-1] through [5-4].

Since SPICE's introduction, a number of new MOSFET levels have been added. The most popular version of SPICE, SPICE 2G.6, has three levels of model complexity. The newest version of SPICE from U.C. Berkeley, (at the time of this writing) SPICE 3F, has 7 levels. The first three are from SPICE 2G.6, plus BSIM1, 2, and 3 (levels 4, 5, 7 (v2) and 8(v3.1)), and MOS6.

SPICE MOSFET Models

Level = 1 Shichman-Hodges
Level = 2 MOS2, Meyer's model [6-5, 11]
Level = 3 MOS3, Semiempirical model [6-1, 11]
Level = 4,5 BSIM, Berkeley short channel IGFET [6-6,7,9]
Level = 6 Sakurai-Newton [6-10]
Level = 7 BSIM3 v2.0, Level = 8 BSIM3 v3.1

Level 1

The level 1 model is useful for quick and approximate measurements. It has the best simulation speed, but it is usually not precise enough because the theory is too approximate and the number of parameters is too small.

The DC characteristics are determined by the nonlinear current source, ID. The value of ID is obtained from the equation proposed by Shichman and Hodges reference [5-4]. The drain current equations are determined by the five model parameters VTO, Beta (KP*W/L), Lambda, Gamma, and Phi. The DC characteristics are the same as the JFET with the exception of the voltage dependent threshold voltage, VTE. Enhancement P and N channel models will have a positive threshold voltage. Depletion P and N channel models have a negative threshold voltage.

Forward Region, VDS > 0

$$VG - VTO < 0: \quad ID = 0$$

$$0 < VGS - VTO < VDS: \quad ID = KP * \frac{W}{L} * (VGS - VTE)^2 * (1 + LAMBDA * VDS)$$

$$0 < VDS < VGS - VTO: \quad ID = KP * \frac{W}{L} * VDS * (2 * (VGS - VTE) - VDS) * (1 + LAMBDA * VDS)$$

Reverse Region:

$VG - VTO < 0$: $ID = 0$

$0 < VGS - VTO < -VDS$: $ID = -KP * \frac{W}{L} * (VGS - VTE)^2 * (1 - LAMBDA * VDS)$

$0 < -VDS < VGS - VTO$: $ID = KP * \frac{W}{L} * VDS * (2 * (VGS - VTE) - VDS) * (1 - LAMBDA * VDS)$

where:

$VTE = VTO + GAMMA * \left(\sqrt{PHI - VBS} - \sqrt{PHI}\right)$

PHI typically ranges from .4 to .8 Volts and GAMMA ranges from .5 to 1.5. For discrete MOSFETs, the substrate is usually connected internally to the source, making the substrate modulation model unnecessary. The diodes in the MOSFET model are not coupled as in the BJT model, giving incorrect results when the substrate is forward biased, as might occur in discrete MOSFET power circuits. KP is used in the MOSFET parameter list, along with W and L, in place of BETA.

Dynamic parameters are determined by the capacitors. The capacitors across the diodes, CBD and CBS use the nonlinear diode equations. The three gate capacitors, CGD, CGS and CGB are linear capacitors in level 1 unless the parameter TOX is specified, in which case the capacitance model proposed by Meyer [6-5] is used. They are derived from the values of CGSO, CGDO, and CGBO which represent overlap capacitances. The level 1 model is usually not used to describe integrated circuit devices because it is too inaccurate.

Level 2

The level 2 model makes corrections to the level 1 model in order to account for effects which aren't in the basic theory. In SPICE 2, the level 2 and 3 MOSFETs contain two built-in models for charge storage effects. The first is the piece-wise linear voltage dependent capacitance model proposed by Meyer [5-5]. The second is the charge controlled model proposed by Ward and Dutton [5-8]. The XQC parameter is used to choose which model will be used. In IsSPICE4, which is based on SPICE 3, there is only one model for charge storage effects [5-11]. The XQC parameter is not used or recognized.

The level 2 model uses the most CPU time and can cause a great deal of convergence problems, especially if not properly specified. But it provides correction to simulate effects which are not predicted in the basic model.

Level 3

The level 3 model is used to simulate short channel MOSFETs (up to 2um). The simulation time is slightly less than for level 2, but the average error is about the same. Model parameter calculations are quite complex.

Most silicon foundries will provide you with level 2 or 3 models if you plan to use their services. Virtually all of the parameters come into play when developing a MOSFET model. The DC parameters are usually easy to determine, however, the dynamic parameters are the real test of the model's validity.

Explanations of levels two and three can be found in [6-1] and you should become familiar with this reference if you wish to model MOSFET integrated circuits.

References

[5-1] THE SIMULATION OF MOS INTEGRATED CIRCUITS USING SPICE 2
A. Vladimirescu and S. Liu, ERL memorandum No. ERLM80/7, Electronics Research Laboratory, University of California, Berkeley, Oct. 1980

[5-2] SEMICONDUCTOR MODELING WITH SPICE
P. Antogegnetti and G. Massobrio, McGraw-Hill, Inc, 1988

[5-3] FET MODELING FOR CIRCUIT SIMULATION
D. Divekar, Kluwer Academic Publishers, 1988

[5-4] MODELING AND SIMULATION OF INSULATED-GATE FIELD EFFECT TRANSISTOR SWITCHING CIRCUITS

H. Shichman and D.A. Hodges, IEEE J. Solid State Circuits, vol. SC-3, Sept. 1968

[5-5] MOS MODELS AND CIRCUIT SIMULATION
J. E. Meyer, RCA Rev., 32, 1971

[5-6] SPICE2 IMPLEMENTATION OF BSIM
B.J. Sheu, D.L. Scharfetter, and P.K. Ko, ERL Memo No. ERL M85/42, Electronics Research Laboratory, U.C. Berkeley, May 1985

[5-7] A MOS PARAMETER EXTRACTION PROGRAM FOR THE BSIM MODEL
J.R. Pierret, ERL Memo No. ERL M84/99 and M84/100, Electronics Research Laboratory, U.C. Berkeley, Nov. 1984

[5-8] A CHARGE-ORIENTED MODEL FOR MOS TRANSISTORS CAPACITANCES
D.E. Ward, R.W. Dutton, IEEE J. Solid-State Circuits, SC-13, 1978

[5-9] DESIGN AND MODELING OF DEEP-SUBMICROMETER MOSFETS
Min-Chie Jeng, ERL Memo No. ERL M90/90, Electronics Research Laboratory, U.C. Berkeley, Oct. 1990

[5-10] A SIMPLE MOSFET MODEL FOR CIRCUIT ANALYSIS AND ITS APPLICATION TO CMOS GATE DELAY ANALYSIS AND SERIES-CONNECTED MOSFET STRUCTURE
T. Sakurai and A.R. Newton, ERL Memo No. ERL M90/19, ERL, U.C. Berkeley, March 1990

[5-11] ANALYSIS OF PERFORMANCE AND CONVERGENCE ISSUES FOR CIRCUIT SIMULATION
Thomas L. Quarles, ERL Memo No. ERL M89/42, Electronics Research Laboratory, U.C. Berkeley, April 1989

Chapter 6 - Macromodels

Operational Amplifier Models

Operational Amplifiers, or Op-amps, can be modeled in a number of ways. The simplest op-amp is a voltage controlled voltage source which has the desired gain, while the most complex model uses the actual integrated or discrete circuit topology. The disadvantages of a complex model are that the analysis of a circuit with several amplifiers may use all the memory available in your computer, use excessive run time and require process information that the IC manufacturer holds proprietary. The simple model may not show important nonlinearities or other second order effects.

Intusoft models are separated into libraries which represent two levels of complexity. The least complex models are good for a first cut analysis and require the smallest number of nodes. These models are in the LIN.LIB file. More complex models, in the NONLIN.LIB file, have more nodes. They require longer simulation time, while yielding a more complete description of the device. Refer to the Extended Syntax chapter of the IsSpice4 User's Guide to see how the different libraries can be included in your file.

IsSpice4 accepts all commonly available vendor supplied op-amp and IC models.

The nonlinear models provided in NONLIN.LIB are hybrids. They duplicate part of the circuit topology to reproduce input and output nonlinearities, while simplifying the bias and interstage circuitry. Hybrid models are a compromise between the simple model and a complete simulation. The subcircuit macro model which is used for op-amp simulation was developed by Intusoft. It is superior to the popular BOYLE op-amp model used by a number of SPICE model vendors. The Intusoft model solves a number of BOYLE model deficiencies, uses fewer components, is more easily adaptable to various op-amps, and simulates more efficiently and accurately.

Generic Op-amps

The Intusoft model libraries contain a number of models for commonly used op-amps. Other op-amp models are also available from various op-amp vendors. To obtain these models, contact Intusoft.

There are also several generic models. The generic models are equation-based subcircuit macros that can simulate hundreds of op-amps just by the specification of a few data sheet parameters. Generic models are possible because characteristics which are common to many op-amps can be modeled using similar techniques. There are generic models for op-amps that are constructed using bipolar and JFET technology, and for current feedback op-amps using 5 or 15 volts. These models are in the linear and nonlinear libraries. The library models for the generic op-amp subcircuits are called OPAMP (Bipolar front end), and FETAMP (JFET front end). The subcircuit names are the same in both libraries. This allows the designer to utilize either a complex or simple model just by altering the *INCLUDE statement. The current feedback op-amps are called AMPC5 (5 volt current feedback) and AMPC15 (15 volt current feedback) and are in the nonlinear library. Parameter passing is used to automatically calculate the IsSPICE4 model parameters, based on the following list of commonly available data sheet parameters:

Data Sheet Value	Parameter
Bandwidth	FT
*Slew Rate Limit	DVDT
Bias Current	IBIAS
Offset Current	IOS
Offset Voltage	VOS
DC Gain	GAIN
*Bandwidth (-3dB)	FC
*Feedback Resistor	RF

* Used for current feedback op-amp

Example: XAMP 1 2 3 4 5 OPAMP {FT=5MEGHz DVDT=5E6
+IBIAS=1NA IOS=1NA VOS=200UV GAIN=150E3}

The nonlinear JFET front end model requires FT, DVDT, VOS, and GAIN. The linear JFET model requires the parameters FT, VOS, and GAIN, while the Bipolar model requires specification of FT, IOS, VOS, IBIAS, and GAIN. The op-amp connections in the order that they must be specified are: (-) inverting input, (+) non-inverting input, output, VCC (+ supply), and VEE (- supply). The current feedback op-amps require the parameters FC, DVDT and RF. The connections as they appear in the subcircuit netlist are: (-) inverting input, (+) non-inverting input, output, VCC (+ supply), and VEE (- supply). See the "SPICE APPLICATIONS HANDBOOK" for a detailed explanation of the current feedback op-amp.

Many other parameters could have been specified, however a lengthy parameter list would discourage use of the generic model. These models have a strong technology and circuit design dependence which constrains meaningful parameter values to be in the neighborhood of those found in vendor data sheets.

Besides modeling the linear and DC transfer function, the nonlinear generic model includes the following characteristics:

- Input Stage Nonlinearities
- Input Voltage and Current Offsets and Bias
- Slew Rate Limiting
- Common Mode Gain
- Power Supply Rejection
- Output Current Limiting
- Output Voltage Limiting
- Reflection of Load Current to Power Input
- Output Stage Nonlinearities

The equivalent circuit shown in Figure 1 takes advantage of the idealized device behavior which is possible through simulation. Parameters are defined for the three stages of the simulated amplifier.

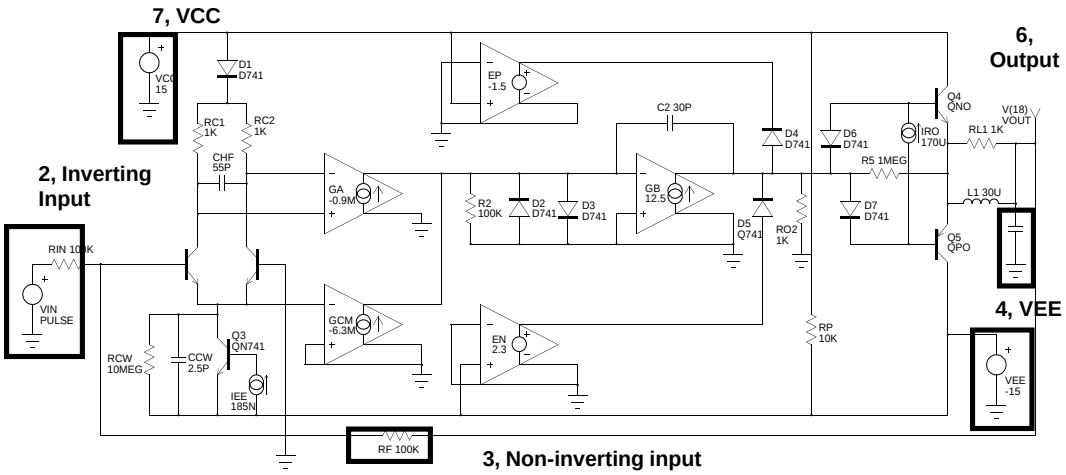


Figure 1, A generic nonlinear op-amp equivalent circuit. Shaded areas contain components which are external to the actual op-amp model and are used for simulation purposes only.

Input Stage

The input nonlinearities are simulated using Q1, Q2, Q3 and D1. These are setup to simulate the topology for a 741 or similar amplifier with respect to bias and common mode range. The input transistors, Q1 and Q2, should be modeled to reflect the performance characteristics of the op-amp so that bias current, offset current and offset voltage are modeled. Noise parameters can also be modeled in this stage by changing the values for AF and KF in the input BJT model QNI1. RCM and CCM will convert common mode signals to differential signals and also couple power line variations into the input. The high frequency pole is modeled with RC1, RC2 and CHF. Values of RC1 and RC2 must be small in order to get the input capacitance of Q1 and Q2 to provide reasonable high frequency behavior. Q1 and Q2 are made slightly different to develop input offsets, and their emission coefficients can be selected to simulate the effect of other transistor cascades in the input and slew rate limiting.

Slew rate limiting is set by this input stage. The large signal output voltage is limited to BETA3 ∗ IEE ∗ RC and the small signal gain is RC ∗ .5 ∗ BETA3 ∗ IEE / (N ∗ VT). If the small signal output is integrated to provide a unity gain crossover at the radian frequency, WT, then the slew rate is:

$$\text{Slew Rate, } \frac{dV}{dt} = 2 * N * VT * WT \qquad \text{Eq. 6.1}$$

The emission coefficient, N, then sets the slew rate limit. Alternatively, you could add emitter resistance as is done in some other models, however, modifying N uses fewer nodes. To make the slew limit unsymmetrical, you can unbalance the collector resistances RC1 and RC2. Note that slew rate limiting is closely related to physical parameters and front end topology as shown in equation 6.3. The emission coefficient of the front end is used to control bandwidth, while bias current controls the slew rate. Slew rate should be within an order of magnitude of the FT to prevent unusual circuit behavior.

Interstage

Controlled sources GA and GCM couple the differential and common mode signals to the interstage amplifier, GB. The DC gain is given by:

$$A_{diff} = RC * 0.5 * \left(\frac{BETA3 * IEE}{N * VT} \right) * GA * R2 * GB * RO2 \qquad \text{Eq. 6.2}$$

At frequencies below the pole at W = 1/(2 ∗ RC ∗ CHF), the gain is given by:

$$A_{diff}\,(mid \quad freq.) = RC * 0.5 * \left(\frac{BETA3 * IEE}{N * VT} \right) * \frac{GA}{jW * C2} \qquad \text{Eq. 6.3}$$

and the unity gain frequency is approximated by solving for W when Adiff = 1.

Two nonlinearities are modeled in the interstage. First, the large signal overshoot is limited by diodes D2 and D3. For amplifiers where this is caused by a pair of diodes, the emission coefficients of the diodes can be adjusted. The second nonlinearity is the output swing which is taken as a constant value subtracted from the power rails. D4, D5, EP and EN act as output limiters. It is important to return the limited current to the subcircuit ground node so that the source, GB, does not generate any apparent power. Static power dissipation is modeled using the resistor RP connected across the power lines.

Output Stage

The output stage is modeled using D6, D7, Q4, Q5 and L. The transistors are not given any AC parameters. Instead, a discrete inductor simulates the AC performance while the transistors' (QNO and QPO) BETA and the source IRO account for both current limit and output resistance. This stage will return the load current to the power lines, enabling simulation of certain power stage configurations.

Example Bipolar and JFET Input Op-amps

The 741 op-amp is a high performance monolithic operational amplifier which is used in many of today's electronic products. Fairchild first developed the UA741; the most comprehensive data sheets may be found in the Fairchild Linear Products catalog.

This amplifier model is based on the generic op-amp model. Models are in the LIN.LIB and NONLIN.LIB files. The linear model is shown in Figure 2.

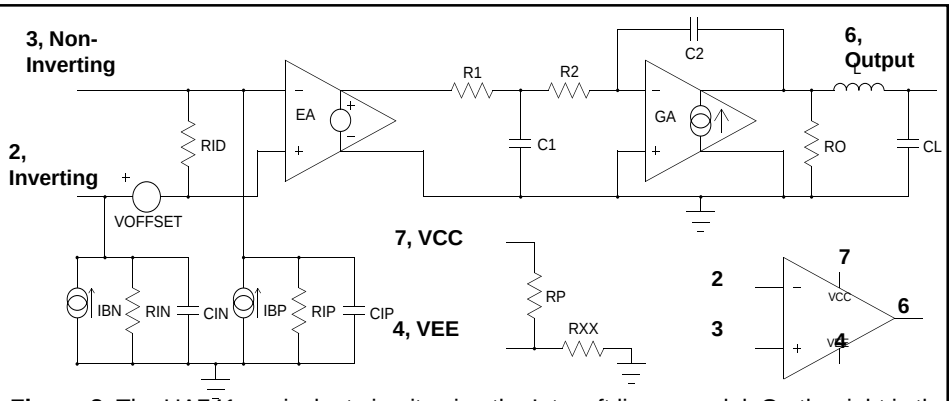


Figure 2, The UA741 equivalent circuit using the Intusoft linear model. On the right is the SPICENET symbol which shows connectivity.

The 156 op-amp was first developed at National Semiconductor under the part number LF156, and features a high impedance JFET front end with relatively fast slew rate and high gain-bandwidth product. The low bias current makes it possible to eliminate bias current compensation resistors; however, its higher bandwidth requires extra care in layout.

Figure 3 defines the topology, and the LIN.LIB and NONLIN.LIB files contain the subcircuit models.

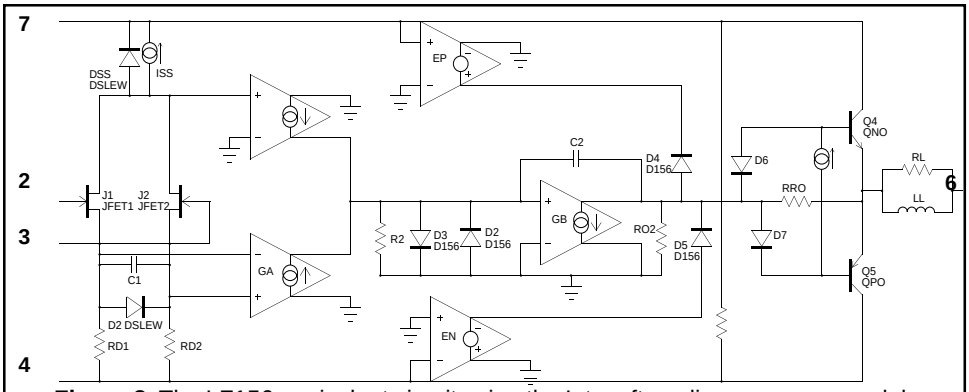


Figure 3, The LF156 equivalent circuit using the Intusoft nonlinear op-amp model.

LM111 Comparator

Comparators are used to convert analog signals to binary levels and use circuitry similar to that used in op-amps. The main difference in circuitry is that stability compensation is eliminated and the output stage is capable of being adjusted to different levels to accommodate a wide range of binary levels. The hybrid models are very similar to op-amps and are therefore included in this section. The 111 comparator was first produced by National Semiconductor as the LM111.

Figure 4 shows the topology, while the parameters are detailed in the Compare.Lib file.

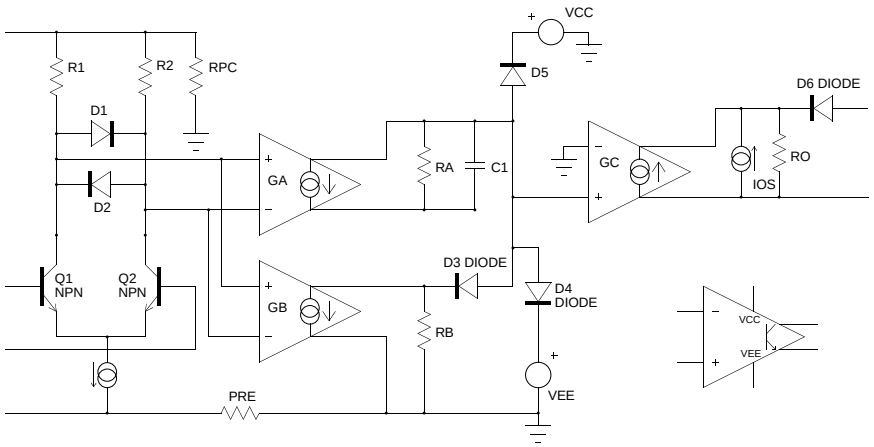


Figure 4, The LM111 equivalent circuit and accompanying SPICENET symbol showing proper comparator connections.

Generic Signal Generators

The signal generators listed below are derived from the standard ISSPICE4 transient signal generators. They are implemented as subcircuits and use the parameter passing feature to make them versatile and easy to use. These subcircuits have defaults for most of the parameters, and unlike the ISSPICE4 transient generators, you may specify the parameters in any order you choose. Shown below is a listing of each source's associated parameters with their defaults, if any, and an example. Parameters without defaults will be marked "ND" and must have a value passed to them.

SIN - *Continuous Sine Wave Voltage*
OFFSET=Voltage Offset (0V), AMP=Peak Amplitude (ND), FREQ=Frequency (ND), DELAY=Starting Delay (0s), DAMP =Damping Coefficient (0)
Example: X1 1 2 SIN {AMP=1 FREQ=10MEG}

PULSE - *Continuous Pulse Train Voltage*
INITIAL=Initial Value (0V), PULSE=Peak pulsed value (ND), DELAY=Starting Delay(0), RISE=Rise Time (ND), FALL=Fall Time (ND), DUTY=Duty Cycle (50%), PERIOD= Waveform Period (ND)

Example: X1 1 2 PULSE {RISE=10N FALL=20N PULSE=5 + DUTY=60 PERIOD=10US}

SAW - *Continuous Sawtooth Voltage*
INITIAL=Initial Value (0V), PULSE=Peak pulsed value (ND), DELAY=Starting Delay (0s), SKEW=Ratio of Pulse rise time to fall time (50), DUTY=Pulse Duty Cycle (50), PERIOD= Waveform Period (ND)
Example: X1 1 2 PULSE {PULSE=10 SKEW=10 DUTY=30 +PERIOD=10K}

AM - *Amplitude Modulated Voltage Waveform*
CARAMP=Peak Carrier Amplitude (ND), CARFQ=Carrier Frequency (ND), MODFQ=Modulation Frequency (ND), PCTMOD =Percent Modulation (ND)
Example: X1 1 2 AM {CARAMP=1 CARFQ=1K MODFQ=10K +PCTMOD=30}

FM - *Frequency Modulated Voltage Waveform*
OFFSET=Offset Voltage (0V), AMP=Peak Amplitude (ND), FREQ=Carrier Frequency (ND), MOD=Modulation index (ND), SIGFREQ=Signal Frequency (ND)
Example: X1 1 2 FM {AMP=5 FREQ=1MEG MOD=1 +SIGFREQ=1MEG}

PSUPPLY - *Power supply*
VCC=Voltage at VCC (12), VEE=Voltage at VEE (-12), VBIAS=Voltage at VBIAS (0)
Example: X1 1 0 2 0 3 0 PSUPPLY {VCC=15 VEE=-15}

VCO - *Voltage Controlled Oscillator*
VPK=Peak Output Voltage (ND), FREQ=Frequency per Volt of Input Control (ND)
Example: X1 1 2 VCO {VPK=10 FREQ=1MEG}

Important Note: In order to use the VCO element, the UIC (Use initial Conditions) keyword must be specified in the .TRAN statement. This allows elements in the subcircuit to be properly initialized. Otherwise, the VCO signal generator will not oscillate properly.

GEN3 - *Three Phase Generator*
FREQ=Output Frequency (ND), VGEN=Peak Output Voltage (ND), MAGERR=Amplitude Unbalance in Percent (ND), PHASE=Phase Disturbance in Degrees (ND)
Example: X1 1 2 3 0 GEN3 {VGEN=10 FREQ=1K MAGERR=0 +PHASE=0}

Phase - *Variable Phase Sin/Cosine Generator*
ANGLE=Sin Wave delay in degrees (0), VGEN=Output Voltage Level (1V), FREQ=Frequency of the output signals (1K)
Example: X1 1 2 3 {ANGLE=45 VGEN=170 FREQ=60}

Phase2 - *Voltage Controlled Phase Sin Generator*
VGEN=Output Voltage Level (1V), FREQ=Frequency of the output signals (1K)
Example: X1 1 2 3 4 {VGEN=170 FREQ=60}

The variable phase Sin/Cosine supply is a variation on the three phase generator macro model. It supplies simultaneous sine, cosine, and variable phase sine wave outputs. The voltage level, frequency, and static phase delay can all be specified by the user. Phase2 is similar to Phase, except that the phase of the sine wave can be varied over time by a user-defined voltage source. The model listings can be found in the SIGNAL.LIB file, along with the rest of the generic sources.

Generic Functions

The generic behavioral function blocks are simple to use. They perform the operation z=f(x,y) where x and y are the inputs, z is the output and f is the function. To use them, all you do is feed a signal in and use the resulting output. The DIVIDER function (voltage divider, z=x/y) is simply a nonlinear dependent source, B element. Be careful to keep the divisor input signal, y, away from the zero neighborhood, otherwise the circuit simulation may abort. The EXP function block, like the DIVIDE, takes advantage of the power of the B element. It performs the exponential function $z=(e^x)$.

A number of other behavioral transfer function blocks are included with your ICAPS package. Check your Model Library Listings booklet for a complete list.

One example using the EXP function is the TANH, hyperbolic tangent function, shown below in Figure 5. It implements the function VOUT = $(e^{(2*VIN)} - 1)/(e^{(2*VIN)} + 1)$. The subcircuit is listed under the name “TANH”. This function can also be implemented using the B element as shown in Figure 5.

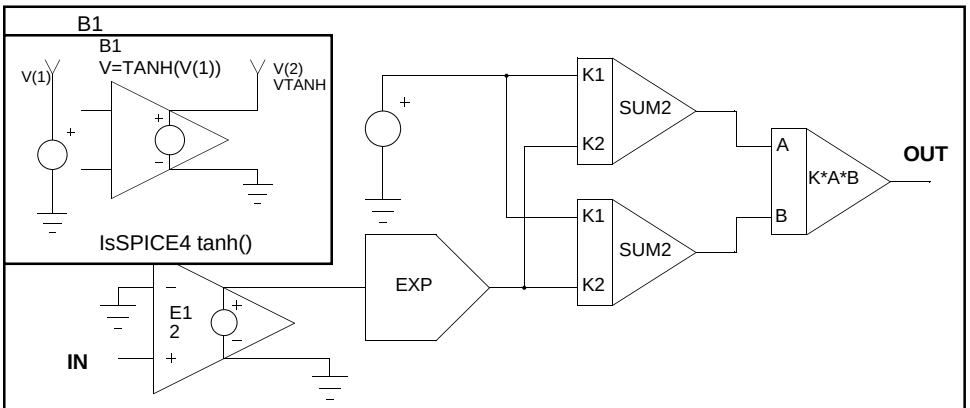


Figure 5, The hyperbolic tangent schematic utilizing the SPICE2 EXP and DIVIDE functions with some analog computer elements, and the IsSPICE4 implementation.

Analog Computer Functions

Analog computer functions, once an important part of computer operations, have given way to the digital computer. However, in terms of analog circuit simulation, analog computer elements have a great deal to offer the circuit designer. Analog computer functions can be used in a number of ways. First, with these functions, IsSPICE4 can be used to solve differential equations such as those encountered in common electrical, mechanical, and physics problems. Second, since the analog computer functions simulate efficiently, they can be used for system analyses. After verification of the system concepts, the various elements can be replaced with the actual circuit topology. Third, they can be used in places where certain functions are required,

but the actual circuit topology need not be used. For example, the next time a summer, multiplier, or integrator function is needed in a design, but the actual circuit is not required, reach for your analog computer library.

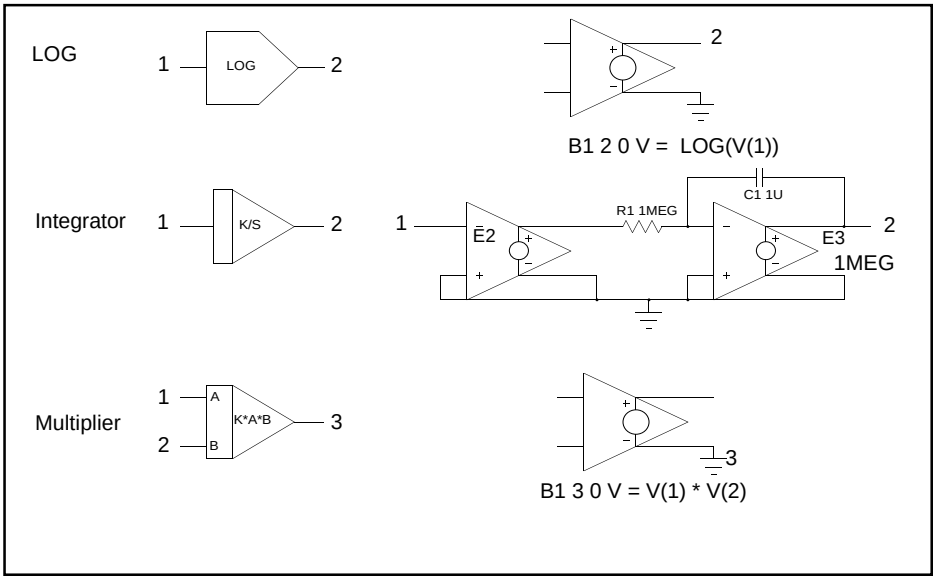


Figure 6, SPICENET symbols for a multiplier, integrator, and logarithmic amplifier are shown to the left, along with the actual ISSPICE4 implementation to the right.

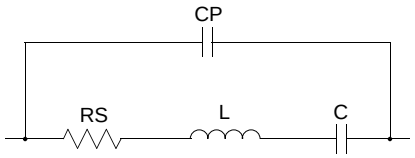
The majority of these are constructed out of dependent sources and basic ISSPICE4 primitive elements. A quick glance at the variety of model listings in Sys.Lib will give you an idea of how useful these elements can be.

Generic Crystals

Example: XOSC 1 2 XTAL {Q=10K RS=10 CP=20PF
+ FREQ=10KHZ}
X2 1 2 XT10

There are no default parameters.

This crystal may be used in oscillator and filter applications. The parameters that are passed to it are the frequency of oscillation (FREQ), Q of the crystal (Q), series resistance (RS) and the parallel capacitance (CP). By specifying the proper parameters, virtually any crystal may be simulated.



$$L = \frac{Q * RS}{2\pi * FREQ}$$

$$C = \frac{1}{Q * 2\pi * FREQ * RS}$$

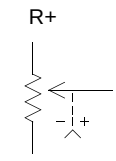
Figure 7, shows the generic crystal model, XTAL.

Generic Potentiometer

Example: X1 1 2 3 4 5 POT {RPOT=50K}
Default RPOT=1K

The voltage controlled resistor uses one parameter, RPOT, which is equal to the potentiometer's total resistance. The output resistance ratio, R1/R2, is controlled by the voltage input K=V(+) - V(-). The control voltage, K, should be kept between 0 and 1. The subcircuit connections are Resistor (+), Resistor(Wiper), Resistor (-), Control (+), and Control (-).

R1 and R2 are variable resistors
R1+R2=RPOT (0<K<1)
R1=K∗RPOT
R2=(1-K)∗RPOT
K=Control voltage, V(+) - V(-)



SPICENET Symbol

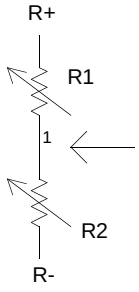


Figure 8, RPOT Model

Opto-Isolator

Example: XLAS 1 2 3 4 5 LN25

The subcircuit is listed in the OPTO.LIB file and the connections are Diode (Anode, Cathode), Transistor (Collector, Base, Emitter).

An OPTO-ISOLATOR consists of a Light Emitting Diode, LED, that is optically coupled to a Bipolar Junction Transistor, BJT. When a current is passed through the diode, light is focused on the base of a photo transistor, causing photo-generated hole electron pairs. We will assume that the light intensity is proportional to current in the diode forward direction, and that most nonlinearities are caused by the BJT current gain, BF. The following equivalent circuit will be used for the IsSpice4 model. The current meter, VM, added in series with the light emitting diode, is used by IsSpice4 to measure input current. The R-C network simulates the LED response.

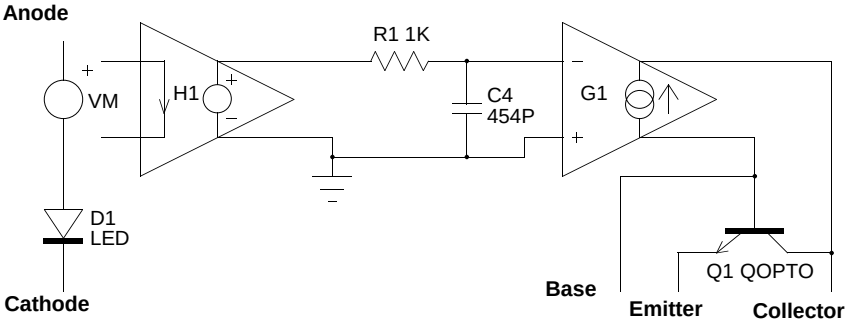


Figure 9, The opto-isolator equivalent circuit

The model parameters will be developed from a composite of the Motorola and Texas Instruments data sheets for the 4N25. First, the LED static parameters are modeled based on the data sheet forward characteristics. These parameters are computed using techniques discussed in the Diode chapter and are:

N = 2
RS = .7
IS = 2.5E-12

The phototransistor static parameters are computed based on a value of Hfe = 325 and a dark current of ID = 8NA given in the data sheet. First, the value of IS is computed as ID/Hfe. Then the value of NF is computed, based on an estimated transistor VBE = .6V and IC = 1MA which results in:

IS = 2.5E-11
NF = 1.3
BF = 325
IKF = 100MA
VAF = 100V

Note the rather unusual approach of computing IS based on reverse characteristics in order to make sure that dark current will be properly simulated. Dark current is very important in establishing the device noise parameters. IKF is used to reflect the loss in isolator gain at high currents. VAF is simply estimated since no data is available in the data sheets.

Next, the LED dynamic characteristics are estimated from data sheet values for CJO = 40PF and rise time, Tr, in the photodiode connected mode of 1USEC. The LED will be assumed to be responsible almost entirely for this parameter so that:

2.3 * R1 * C1 = Tr
R1 = 1K
C1 = 434PF
CJO = 40PF

Next, the phototransistor dynamic parameters are estimated from the phototransistor connected fall time, Tf = 2USEC, for unsaturated operation to compute Ft and then TF. Next, the saturated switching storage time, Ts = 4USEC, and fall time, Tfs=8USEC, are used to compute TR and Cob. BR plays an important part in storage time characteristics and is assumed to have a value of 10.

Ft = Hfe ∗ 2.3 / Tf
TF = 1 / (2 ∗ p ∗ Ft) = .43NS
TR = 1 / BR ∗ Ts / ln[BF/10] = 114NSEC
Cob = Tfs / (2.3 ∗ BF ∗ VCC / ICSAT) = 11PF
CJC = 2 ∗ Cob = 22PF
CJE = 7 ∗ Cob = 77PF

The model description is then:

```
.SUBCKT LN25 1 2 3 4 5
VM 1 6
D1 6 2  LED
H1 7 0  VM  .00154
R1 7 8  1K
C1 8 0  454PF
G1 3 4 8 0  1
Q1 3 4 5 QOPTO
.MODEL  LED  D(N=2 RS=.7 CJO=40PF IS=2.5E-12)
.MODEL  QOPTO  NPN(IS=2.5E-11 NF=1.3 CJC=22PF
+ CJE=77PF TF=.44NS TR=114NS BF=325 BR=10
+ IKF=100MA VAF=100)
.ENDS
```

Parameters VAF, NF, CJE and BR are estimates which could be improved by measurement. Figure 10 illustrates the response using the data sheet circuit for saturated switching. The parameters TR, CJC and CJE were adjusted using simulations to force agreement with the data sheet.

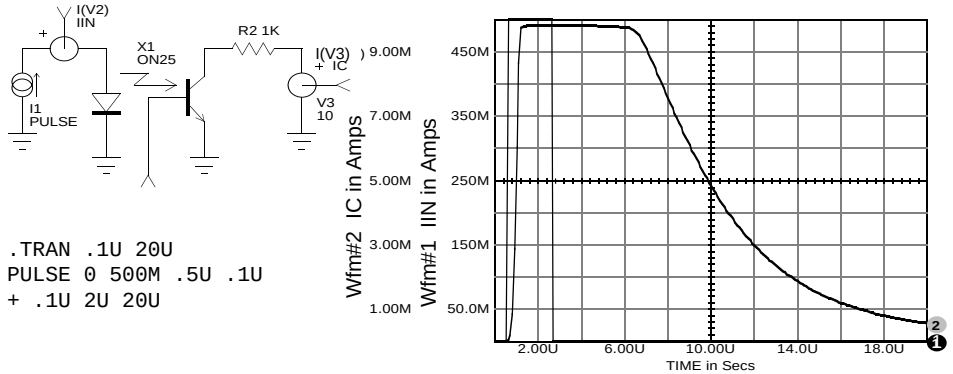


Figure 10, Simulation of the 4N25 shows the turn-on and turn-off response.

Generic Voltage Controlled Resistor

The subcircuit shown below is a model for a simple voltage controlled switch. The generic switch can be used for a wide variety of purposes, especially when general simulations to study circuit or system concepts is being performed. The switch is created using the IsSPICE4 primitive G (voltage controlled current source) tied back onto itself.

```
*OPEN WHEN V(3,0) = 0,
*CLOSED WHEN V(3,0) < > 0
*ON RESISTANCE IS 1 / V(3)
*OFF RESISTANCE IS 1E12
.SUBCKT SWITCH 1 2 3
R1 1 2 1E12
G1 1 2 POLY(2) 1 2 3 0 0 0 0 0 1
.ENDS
```

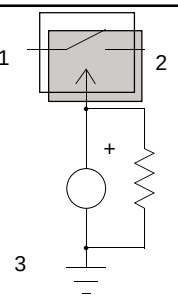


Figure 11, The generic switch netlist and SPICENET switch symbol in the boxed area. The voltage source value controls the resistance between nodes 1 and 2.

The switch is very simple to use. Applying zero volts to the control input opens the switch. The open resistance is 1E12 Ohms. It may be changed, if desired. Applying any voltage to the switch control input, V(3), closes the switch and gives it a resistance of 1/V(3). For example, applying a voltage pulse of 0 to 1 volt to the control input will change the resistance seen from port 1 to port 2 from 1E12 to 1 Ohm. This switch model does not have any hysteresis.

Generic Phase Locked Loop Models

The phase locked loop models are described in Chapter 9 of the "SPICE APPLICATIONS HANDBOOK" [6-7]. The listings for the phase locked loop models can be found in Random.Lib (Random Noise sources), Signal.Lib (Voltage Controlled Oscillator), and Sys.Lib (Filter Blocks) files.

Random Noise Sources

The random noise sources are used to provide a noise signal source for the transient analysis. The subcircuit has only one connection, the signal output. The parameters that must be specified are TIM, the total analysis time, usually TSTOP, and MAG, the RMS magnitude of the noise signal. The noise sources are comprised of piece wise linear (PWL) sources which are stacked in series. RAN1, RAN2 and RAN3 are 128 point noise sources. RAN4 is a 256 point noise source and RAN5 is a 512 point noise source. As more points are used, the the analysis will require more time. The larger point sources will have a higher frequency content than the smaller point sources for the same time span. The random noise sources were built using a random number generator in order to provide the time and voltage multiplication factors.

```
XNOISE 1 RAN4 {TIM=1U MAG=1}

.SUBCKT   RAN4   4
R1  0  1  1K
V1  1   0  PWL  0,{-1.7071*MAG} {00391∗TIM},{0.7963∗MAG},
```

Figure 12, Partial listing of the random noise source shows its generic nature.

Generic Thermal Models

The thermal models found in the THERMAL library are described in the July and October 1988 newsletters. Both *Intusoft Newsletters*, as well as the published paper "Modeling Thermal Effects Using Spice" by L. G. Meares [6-4] are available in the "SPICE APPLICATIONS HANDBOOK" [6-7].

Generic Interconnect

Example: X23 5 7 WIRE {L=1 Z=100}

where: L is the connect length in inches
Z is the transmission line impedance in Ohms

Assumption: L * 125PSEC/inch is small compared to rise/fall time. Propagation velocity is 1 / 125 PSec/inch

The most frequently used element in electronic circuits, the interconnect or “wire”, is rarely modeled. The most computationally efficient model for PC cards, backplanes and thick film substrates is an L-C section of a transmission line. Integrated circuits, with the exception of Microwave IC’s, can be modeled with R-C sections. The generic interconnect presented here is for the L-C case and requires that circuit rise and fall times are long compared to the “wire” length, [6-2]. Microstrip propagation times of 125PSec per inch, [6-3], are built in to the model. Wire wrap backplanes may require several sections or the use of transmission lines. To make efficient use of computer memory, IsSpice4 transmission lines should only be used when the delay time is a large fraction of the analysis time. You may use the following equations to modify the built-in model for different materials and geometries. Impedance for PC cards and thick film substrates is approximated by:

$$Z = 377 * \left(\frac{h}{w}\right) * (Er)^{-0.5}$$

where: h is the height of the conductor above the ground plane
w is the conductor width
Er is the relative dielectric constant

Examples, A PC card has h=.007, w=.025, Er=2: Z=75

Thick film, Alumina: w=.010, h=.001, Er=10: Z=12
(t must be increased to 264 PSec/inch for Alumina)

The impedance for wire wrap is:

$$Z = 138 * (Er)^{-0.5} * \log\left(4 * \frac{h}{w}\right) \qquad [6\text{-}3]$$

Example: w = .1 (include insulation)
h = .25 (average)
Er = 2 (Avg of air and insulation)
Z = 150

To construct a new model, calculate a new value for t based on Er and insert the value in the model. Use one of the above equations for Z which can be passed as a parameter. Alternatively, you can pass ER as a parameter, using the same model for all occasions.

v, the propagation velocity, = c * (Er) $^{-.5}$
t = 1 / v = 125 PSec/inch, built-in

Then, for each L-C Section:

$$L1 = Z * L * t \quad \text{or} \quad = Z * L * t * (Er)^{0.5}$$

$$C1 = t * \frac{L}{Z} \quad \text{or} \quad = t0 * (Er)^{0.5} * \frac{L}{Z}$$

Closed form equations for impedance, given above, should be taken as approximations and supported by measured data. Capacitance is frequently higher than predicted because of fringing and additional dielectric encapsulation.
The validity of an LC approximation to a transmission line requires that the group delay (dPhase/dFreq) is linear for frequencies that contain useful information. Reference 6-2 uses a criteria of 3 * TD < trise/fall. External circuit resistance and your accuracy expectations will also influence this criteria. The following figure shows how accuracy changes with termi-

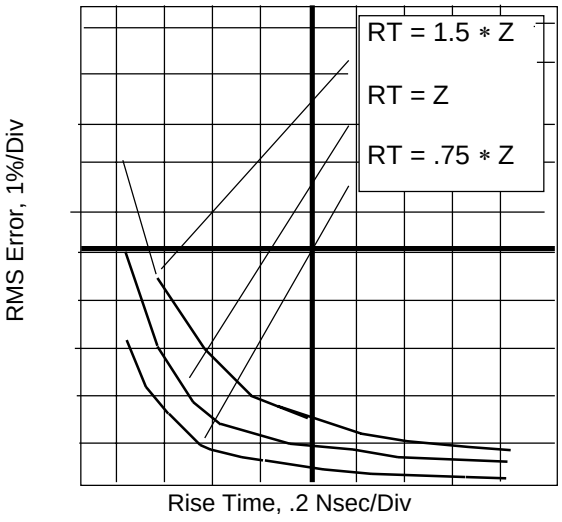


Figure 13, Model error as a function of time and terminating resistance

nating resistance and input rise time for an 8 section transmission line with a 1 nanosecond delay. In this example, each section has a 125 PSec delay. The error shown in the plot is an RMS value over 5 Nsec, resulting from a step input whose rise time is plotted in the X axis.

References

[6-1] PHYSICS OF SEMICONDUCTOR DEVICES
Sze, S.M. AT&T Bell Labs., Murray Hill, NJ
John Wiley & Sons, Copyright 1981, 2nd Edition

[6-2] HYBRID CIRCUIT TECHNOLOGY FOR VHSIC
Lewis, E.T.; Ciccio, J.;Thun,R.E.
Raytheon Co. Missile Systems Div. Bedford MA
1980 Proceeding of the Hybrid Microcircuits Symposium,pp48-83
U.S. Army, ERADCOM, Fort Monmouth, NJ

[6-3] REFERENCE DATA FOR RADIO ENGINEERS
ITT, 5th edition, chapter 22, pp22-26
Howard W. Sams & Co.

[6-4] MODELING THERMAL EFFECTS USING SPICE
Meares, L.G.
PowerCAD, Long Beach, 1988, Originally published intusoft newsletters, July/October 1988

[6-5] SIMULATING WITH SPICE
Meares, L.G., Hymowitz, C.E.
Intusoft 1988

[6-6] ANALOG COMPUTATION
Jackson, A.S.,
McGraw-Hill, 1960

[6-7] SPICE APPLICATIONS HANDBOOK, 2nd Edition
Hymowitz, C.E., Meares, L.G.
Intusoft 1990, 1994

Chapter 7 - Models For Power Electronics

Saturable Reactor Model

A saturable reactor is a magnetic circuit element consisting of a single coil wound around a magnetic core. The presence of a magnetic core drastically alters the behavior of the coil by increasing the magnetic flux and confining most of the flux to the core. The magnetic flux density, B, is a function of the applied MMF, which is proportional to ampere turns. The core consists of a number of tiny magnetic domains which are made up of magnetic dipoles. These domains setup a magnetic flux that adds to or subtracts from the flux which is setup by the magnetizing current. After overcoming initial friction, the domains rotate like small DC motors, to become aligned with the applied field. As the MMF is increased, the domains rotate until they are all in alignment and the core saturates. Eddy currents are induced as the flux changes, thereby causing added loss.

The saturable reactor cannot be modeled using a single IsSpice4 primitive element. Therefore, Intusoft has created a saturable core macro model which utilizes the IsSpice4 subcircuit feature. The saturable core is capable of simulating nonlinear transformer behavior including saturation, hysteresis, and eddy current losses. To make the model even more useful, it has been parameterized. This is a technique which allows the characteristics of the core to be determined via the specification of a few key parameters. At the time of the simulation, the specified parameters are passed into the subcircuit. The equations in the subcircuit (inside the curly braces) are then evaluated and replaced with a value which makes the equation-based subcircuit compatible with IsSpice4.

The parameters that must be passed to the subcircuit include:

Flux Capacity in Volt-Sec (VSEC)
Initial Flux Capacity in Volt-Sec (IVSEC)
Magnetizing Inductance in Henries (LMAG)
Saturation Inductance in Henries (LSAT)
Eddy current critical frequency in HZ (FEDDY)

The saturable core may be added to a model of an ideal transformer to create a complete transformer model. To use the model, just place the core across the transformer's input terminals and specify the parameters. A special subcircuit test point has been provided to allow the monitoring of the core flux. Placing a SPICENET test point symbol on the pin or supplying a dummy netlist node number will allow the designer to get a reading of the internal core flux. Since there are two connections in the subcircuit, no connection is required at the top subcircuit level other than the dummy node number.

A sample ISSPICE4 call to the saturable core subcircuit will look like the following:

```
X1  2  0  3  CORE { VSEC=50U IVSEC=-25U LMAG=10MHY
+ LSAT=20UHY FEDDY=20KHZ }
```

The generic saturable core model is listed below.

```
.SUBCKT CORE 1 2 3
F1 1 2 VM1 1
G2 2 3 1 2 1
E1 4 2 3 2 1
VM1 4 5
RX 3 2 1E12
CB 3 2 {VSEC/500}
+ IC={IVSEC/VSEC*500}
RB 5 2 {LMAG*500/VSEC}
RS 5 6 {LSAT*500/VSEC}
VP 7 2 250
D1 6 7 DCLAMP
VN 2 8 250
D2 8 6 DCLAMP
.MODEL DCLAMP D(CJO={3*VSEC/
+ (6.28*FEDDY*500*LMAG)} VJ=25)
.ENDS
```

Subcircuit Netlist

To make the netlist ISSPICE4 compatible, just replace all of the equations in the curly braces with numerical values.

How The Core Model Works

Modeling the physical process performed by a saturable core is most easily accomplished by developing an analog of the magnetic flux. This is done by integrating the voltage across the core and then shaping the flux analog with nonlinear elements to cause a current flow which is proportional to the desired function. This gives good results when there is no hysteresis, as illustrated in Figure 1.

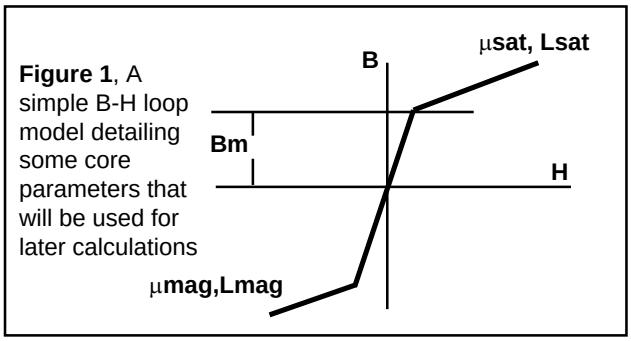


Figure 1, A simple B-H loop model detailing some core parameters that will be used for later calculations

The input voltage is integrated using the voltage controlled current source, G, and the capacitor CB. An initial condition across the capacitor allows the core to have an initial flux. The output current from F is shaped as a function of flux using the

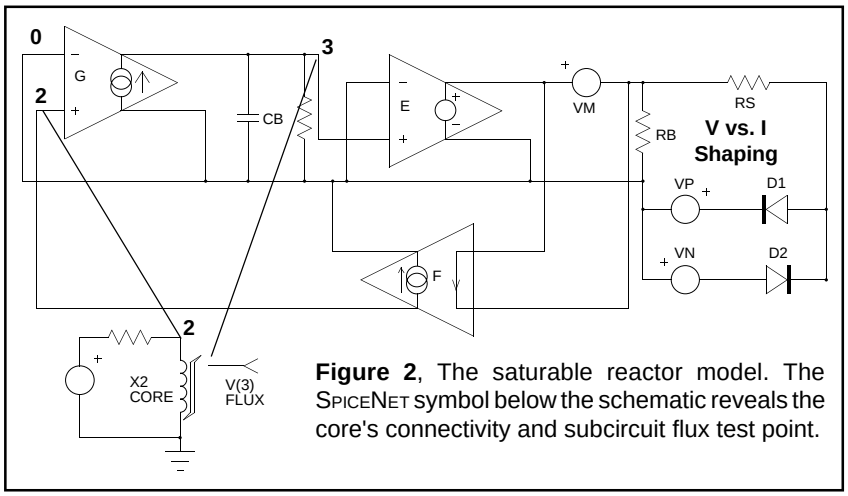


Figure 2, The saturable reactor model. The SPICENET symbol below the schematic reveals the core's connectivity and subcircuit flux test point.

voltage sources VN and VP and diodes D1 and D2. The inductance in the high permeability region is proportional to RB, while the inductance in the saturated region is proportional to RS. Voltage VP and VN represent the saturation flux. Core losses can be simulated by adding resistance across the input terminals; however, another equivalent method is to add capacitance across resistor RB in the simulation. Current in this capacitive element is differentiated in the model to produce the effect of resistance at the terminals. The capacitance can be made a nonlinear function of voltage which results in a loss term that is a function of flux. A simple but effective way of adding the nonlinear capacitance is to give the diode parameter, CJO, a value, as is done here. The other option is to use a nonlinear capacitor across nodes 2 and 6, however, the capacitor's polynomial coefficients are a function of saturation flux, causing their recomputation if VP and VN are changed.

Losses will increase linearly with frequency, simulating high frequency core behavior. A noticeable increase in MMF occurs when the core comes out of saturation, an effect that is more pronounced for square wave excitation than for sinusoidal excitation, as shown in Figure 3. These model properties agree closely with observed behavior [7-2]. The model is setup for orthonol and steel core materials which have a sharp transition from the saturated to the unsaturated region. For permalloy cores, the transition out of saturation is less pronounced. To account for the different response, the capacitance value in the diode model (CJO in DCLAMP), which affects core losses, should be scaled down. Also, scaling the voltage sources VN and VP down will soften the transition.

The DC B-H loop hysteresis, usually unnecessary for most applications, is not modeled because of the extra model complexity, causing a prediction of lower loss at low frequencies. The hysteresis, however, does appear as a frequency dependent function, as seen on the previous page, providing reasonable results for most applications, including magnetic amplifiers. The model shown in Figure 2 simulates the core characteristics and takes into account the high frequency losses associated with eddy currents and transient widening of the B-H loop caused by magnetic domain angular momentum.

Losses will increase linearly with frequency, simulating high frequency core behavior.

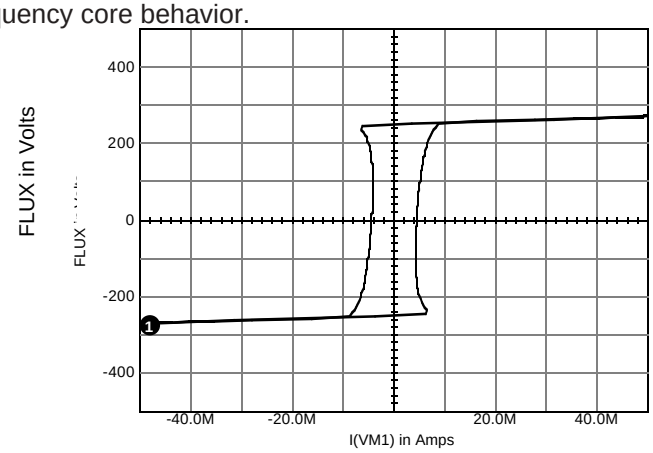
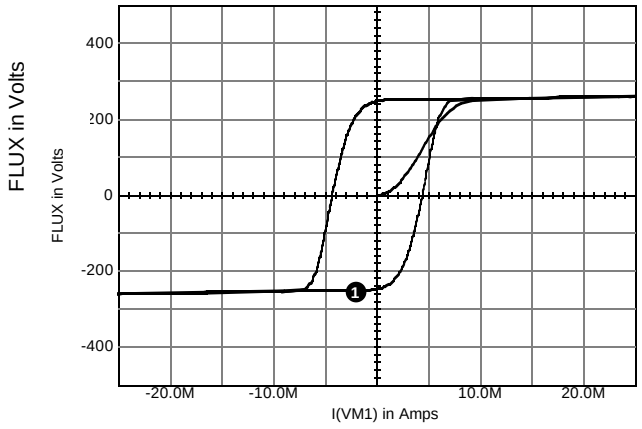


Figure 3, The saturable core model is capable of being used with both Sine (Below) and Square (Above) wave excitation.



Calculating Core Parameters

The saturable core model is setup to be described in electrical terms, thus allowing the engineer to design the circuitry without knowledge of the core's physical makeup. After the design is completed, the final electrical parameters can then be used to calculate the necessary core magnetic/size values. The core model could be altered to take as its input magnetic and size parameters. The core could then be described in terms of N, Ac,

Ml, μ, and Bm and would be more useful for studying previously designed circuits. But the electrical based model is better suited to the natural design process. The saturable core model's behavior is defined by the set of electrical parameters, shown in Figure 1 and Figure 4. The core's magnetic/size values can be easily calculated from the following equations which utilize cgs units.

Parameters Passed To Model

VSEC	Core Capacity in Volt-Sec
IVSEC	Initial Condition in Volt-Sec
LMAG	Magnetizing Inductance in Henries
LSAT	Saturation Inductance in Henries
FEDDY	Frequency when LMAG Reactance = Loss Resistance in Hz

Equation Variables

Bm	Maximum Flux Density in Gauss
H	Magnetic Field Strength in Oersteds
Ac	Area of the Core in cm^2
N	Number of Turns
Ml	Magnetic Path Length in cm
μ	Permeability

Faraday's law, which defines the relationship between flux and voltage is:

$$E = \frac{d\varphi}{dt} * 10^{-8} \qquad \text{Eq. 7.1}$$

where E is the desired voltage, N is the number of turns and j is the flux of the core in maxwells. The total flux may also be written as:

$$\varphi_T = 2 * Bm * Ac \qquad \text{Eq. 7.2}$$

Then, from 1& 2,

$$E = 4.44 * Bm * Ac * F * N * 10^{-8}$$

Eq. 7.3

and

$$E = 4.0 * Bm * Ac * F * N * 10^{-8}$$

Eq. 7.4

where Bm is the flux density of the material in Gauss, Ac is the effective core cross sectional area in cm^2, and F is the design frequency. Equation 7.3 is for sinusoidal conditions while equation 7.4 is for a square wave input. The parameter VSEC can then be determined by integrating the input voltage resulting in:

$$\int edt = N\varphi_T = N * 2 * Bm * Ac * 10^{-8} = VSEC$$

Eq. 7.5

also from E = L di/dt we have,

$$\int edt = Li$$

Eq. 7.6

The initial flux in the core is described by the parameter **IVSEC**. To use the IVSEC option, you must put the UIC keyword in the ".TRAN" statement. The relationship between the magnetizing force and current is defined by Ampere's law as

$$H = 0.4 * \pi * N * \frac{i}{Ml}$$

Eq. 7.7

where H is the magnetizing force in oersteds, i is the current through N turns, and Ml is the magnetic path length in cm.

From equations 8.5, 8.6, and 8.7 we have

$$L = N^2 * Bm * Ac * \left(\frac{0.4 * \pi * 10^{-8}}{H * Ml} \right)$$

Eq. 7.8

with μ = B/H we have

$$L(mag, sat) = \mu(mag, sat) * N^2 * Bm * 0.4 * \pi * 10^{-8} * \frac{Ac}{Ml}$$

Eq. 7.9

The values for LMAG and LSAT can be determined by using the proper value of μ in Eq. 7.9. The values of permeability can be found by looking at the B - H curve and choosing two values for the magnetic flux, one value in the linear region where the permeability will be maximum, and one value in the saturated region. Then, from a curve of permeability versus magnetic flux, the proper values of m may be chosen. The value of μ in the saturated region will have to be an average value over the range of interest. The value of FEDDY, the eddy current critical frequency, can be determined from a graph of permeability versus frequency, as shown in Figure 4. By choosing the approximate 3db point for μ, the corresponding frequency can be determined.

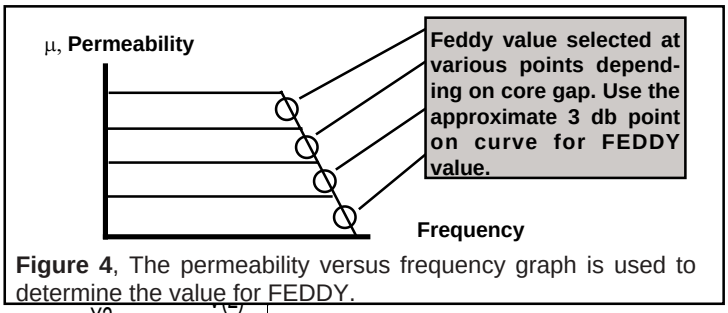


Figure 4, The permeability versus frequency graph is used to determine the value for FEDDY.

Using And Testing The Saturable Core

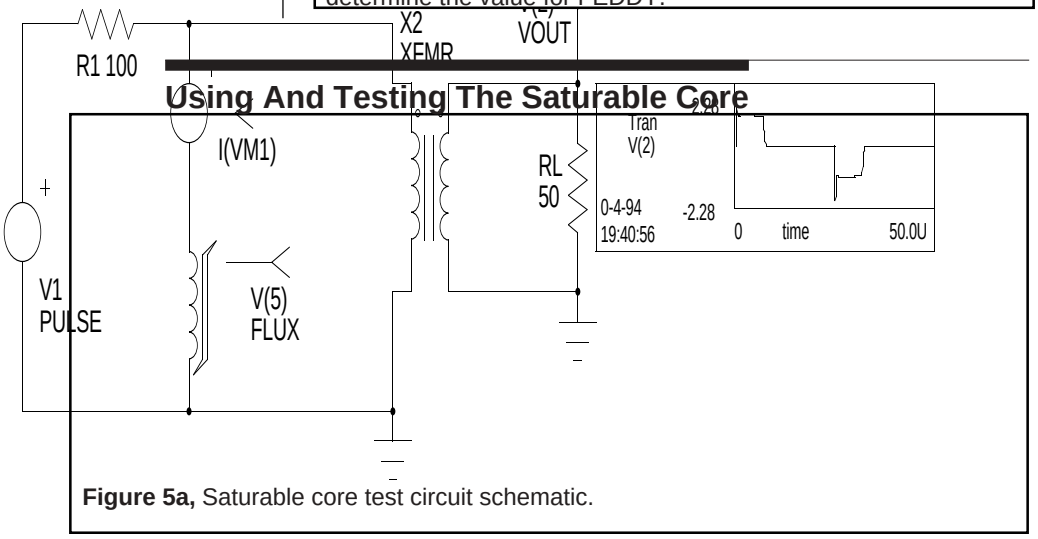


Figure 5a, Saturable core test circuit schematic.

```
Saturable core Test Circuit
.OPTIONS LIMPTS=1000
*SPICE_NET
.TRAN .1US 50US
*INCLUDE DEVICE.LIB
.OPTIONS LIMPTS=1000
*ALIAS  V(3)=VOUT
*ALIAS  V(5)=FLUX
*ALIAS  V(4)=VIN
.PRINT TRAN V(3)  V(5)  I(VM1) V(4)
R1 4 2 100
R2 3 0 50
X1 1 0 5 CORE {VSEC=25U
+IVSEC=-25U LMAG=10MHY
+ LSAT=20UHY FEDDY=25KHZ}
X2 2 0 3 0 XFMR  {RATIO=.3}
VM1 2 1
V2 4 0 PULSE -5 5 0US 0NS 0NS
+25US
*Use the above statement for
*Square wave excitation
*V2 4 0 SIN 0 5 40K
*Use the above statement for Sin
*wave excitation
*Adjust Voltage levels to insure core
*saturation
.END
```

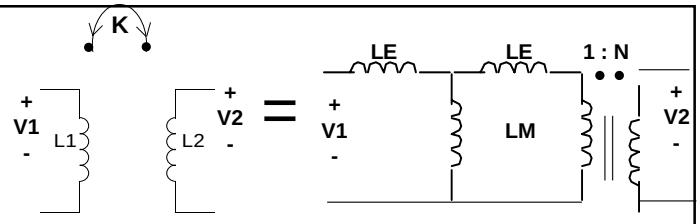
Figure 5b, Saturable core test circuit netlist.

The test circuit shown in Figure 5 can be used to evaluate a saturable core model. Specify the core parameters in the curly braces and adjust the voltage levels in the “V2 4 0 PULSE” or “V2 4 0 SIN” statements to insure that the core will saturate. You can use Eq.7.3 and 7.4 to get an idea of the voltage levels which are necessary to saturate the core. The .TRAN statement may also need adjustment, depending on the frequency specified by the V2 source. You can use the preprocessing programs INCLUDE and PARAM to get the subcircuit out of the Intusoft device model library and evaluate the parameterized model, or it may be done manually. The core parameters must remain reasonable or the simulation may fail. After simulation, plotting V(5) versus I(VM1) (Flux vs. Current through the core) will result in a B-H plot.

Transformer Models

The usual method of simulating a transformer using IsSPICE4 is by specifying the open circuit inductance seen at each winding and then adding the coupling coefficients to a pair of coupled inductors. This technique tends to lose the physical meaning associated with leakage and magnetizing inductance and does not allow the insertion of a nonlinear core. It does, however, provide a transformer that is simple to create and simulates efficiently. The coupled inductor type of transformer, its related equations and relationship to an ideal transformer with added

leakage and magnetizing inductance is shown in Figure 6.



$$V1 = L1\frac{di1}{dt} + M\frac{di2}{dt}$$

$$V2 = M\frac{di1}{dt} + L2\frac{di2}{dt}$$

$$M = K\sqrt{L1 * L2}$$

If K = 1

$$L1 = LM$$

$$L2 = N^2 * L1$$

$$K = 1 - \frac{LE}{LM}$$

Figure 6, The coupled inductor transformer, left, is computationally efficient, but it cannot provide access to LE and LM or be used as a building block. The ideal transformer with discrete inductances and their relationship to the coupling coefficient is shown on the right.

In order to make a transformer model that more closely represents the physical processes, it is necessary to construct an ideal transformer and model the magnetizing and leakage inductances separately. The ideal transformer is one that preserves the voltage and current relationships, shown in Figure 7, and has a unity coupling coefficient and infinite magnetizing inductance. The ideal transformer, unlike a real transformer, will operate at DC, a property which is useful for modeling the operation of DC-DC converters.

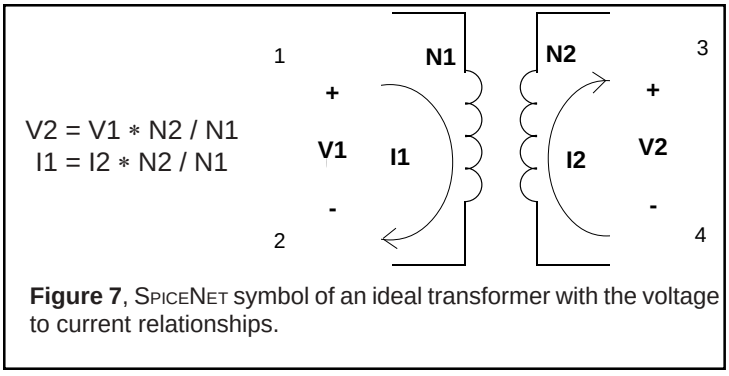


Figure 7, SPICENET symbol of an ideal transformer with the voltage to current relationships.

The coupling coefficient of a transformer wound on a magnetic core is nearly unity when the core is not saturated and depends on the winding topology when the core is saturated. The work of Hsu, Middlebrook and Cuk [7-3] develops the relationship of leakage inductance, showing that relatively simple measurements of input inductance with shorted outputs yield the necessary model information.

Multi-winding topologies can be simulated by using combinations of this 2 port representation. (See the *Intusoft Newsletter* Feb. 1989, Page 9). The IsSpice4 equivalent circuit is shown in Figure 8 and implements the following equations:

$$V1 * RATIO = V2 \qquad I1 = I2 * RATIO$$

RP and RS are used to prevent singularities in applications where terminals 1,2 are open circuit or terminals 3,4 are connected to a voltage source. RATIO is the turns ratio from winding 1,2 to winding 3,4. Polarity "dots" are as shown on terminals 1 and 3.

```
.SUBCKT XFMR 1 2 3 4
E  5  4  1  2  {RATIO}
F  1  2  VM  {RATIO}
VM  5  6
RP  1  2  1MEG
RS  6  3  1U
.ENDS
```

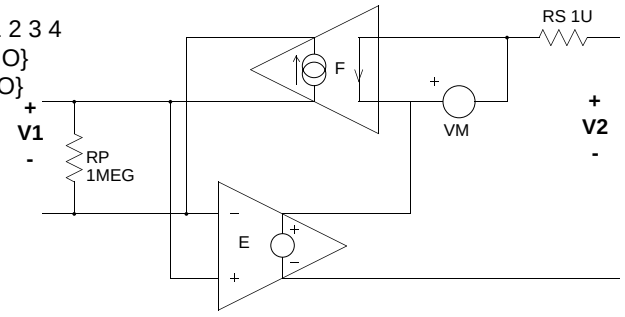


Figure 8, The Intusoft ideal transformer model allows operation at DC and the addition of magnetizing and leakage inductances, as well as a saturable core to make a complete transformer model. Parameter passing allows the transformer to simulate any turns ratio.

The magnetizing inductance is added by placing the saturable reactor model across any one of the windings. Coupling coefficients are inserted in the model by adding the series leakage inductance for each winding as shown in Figure 9.

The leakage inductances are measured by finding the short circuit input inductance at each winding and then solving for the individual inductance. These leakage inductances are independent of the core characteristic shown by ref [7-3]. The final model, incorporating the CORE and XFMR subcircuits along with the leakage inductance and winding resistance is shown in Figure 9.

IsSPICE4 models cannot represent all possible behavior because of the limits of computer memory and run time. This model, as most simulations, does not represent all cases.

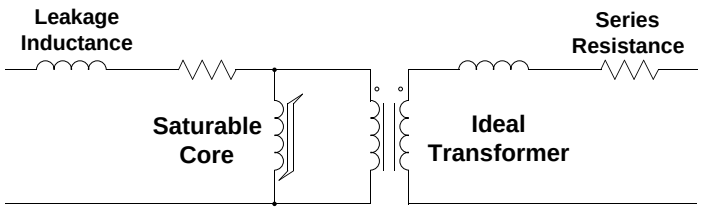


Figure 9, A Complete Transformer Model. The saturable core may be combined with the ideal transformer, XFMR, and some leakage inductance and series resistance to create a complete model of a transformer.

Modeling the core in Figure 9 as a single element referred to one of the windings works in most cases; however, some applications may experience saturation in a small region of the core, causing some windings to be decoupled faster than others, invalidating the model. Another limitation of this model is for topologies with magnetic shunts or multiple cores. Applications like this can frequently be solved by replacing the single magnetic structure with an equivalent structure using several transformers, each using the model presented here.

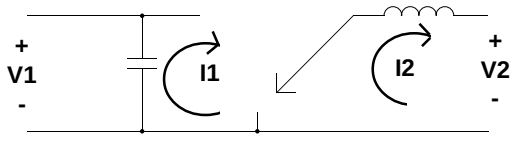
Small Signal AC Analysis of PWMs

SPICE has generally been perceived as being weak in its ability to model the small signal behavior of switching circuits. The AC analysis will reduce a circuit to a linear small signal representation about its large signal operating point. This process does not properly model the pulse width modulator in a switching power supply.

The ideal transformer that has been developed can be seen intuitively as a power supply model. Operating at DC, it will preserve the input-output relationships of filter networks and can be used for control simulation by adding the small signal control parameters. This has been done for Buck, Boost, Buck-Boost and Cuk topologies under the restriction of continuous conduction.

To develop the rationale for the PWM model, the state averaging technique of Middlebrook [7-4] is applied to a Buck regulator shown in Figure 10. In this approach, the nodal equations are used rather than the state equations in a manner that will cause the states, inductor current and capacitor voltage, to be averaged over the two switch positions.

These results are then rearranged to form the equivalent circuit shown in Figure 11. Lower case symbols in Figure 11 are used to represent small signal parameters and upper case symbols are used for large signal parameters.



V2 = D ∗ V1, averaged by L
I1 = D ∗ i2, averaged by C

Figure 10, Buck regulator

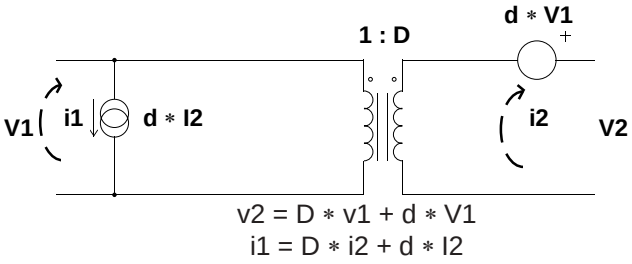


Figure 11, Small signal equivalent Buck regulator model.

The model shown in Figure 11 can be used to replace the pulse width modulator switches for the small signal analysis. Notice, however, that this model is exactly the small signal model of the ideal transformer if the turns ratio were used to replace the duty ratio.

The POLY directive in IsSpice4 can be used to create a new transformer model in which turns ratio is a controlled variable. IsSpice4 will then compute the small signal parameters and automatically make the small signal model. Moreover, this model produces correct large signal response, enabling the designer to study start up or pulsed line and load response without resorting to a complete pulse width modulator simulation.

The new IsSpice4 model, shown in Figure 12a, is an electrically adjustable transformer, which is precisely the definition of the switching element used in pulse width modulators.

Large signal behavior can also be simulated with this new model as long as the continuous conduction restriction is applied. In the context of this model, continuous conduction is required to keep the switches in their predefined positions. For circuits using a free wheeling diode as a switch, it is necessary for the inductor current to continue in the same direction for the switch to behave as modeled. Forced switch commutation, for example, using a MOSFET switch instead of a diode, would remove the restriction.

Figure 13 is the schematic of a Cuk regulator. Other canonical forms are given in reference [7-5].

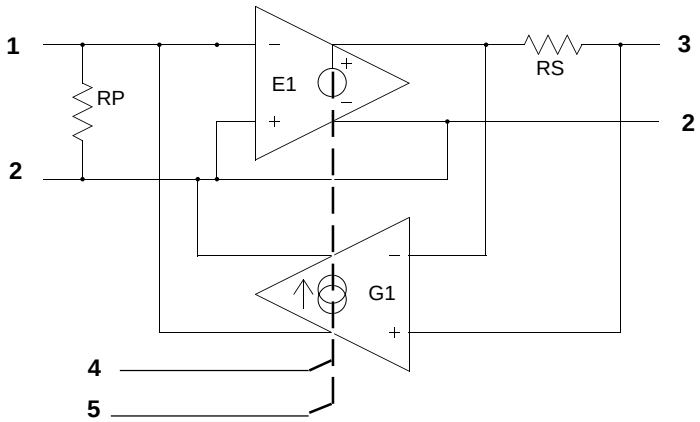


Figure 12a, Pulse Width Modulator (PWM) equivalent circuit. Dashed line indicates that the voltage V(4,5) controls the dependent sources G1 and E1.

```
*Pulse Width Modulator
.SUBCKT PWM 1 2 3 4 5
E 6 2 POLY(2) 1 2 4 5 0 0 0 0 1
G 1 2 POLY(2) 6 3 4 5 0 0 0 0 1K
RP 1 2 1MEG
RS 3 6 1M
.ENDS
```

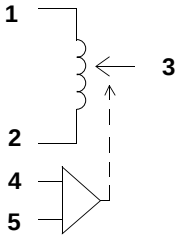


Figure 12b, Pulse Width Modulator (PWM) symbol and subcircuit netlist.

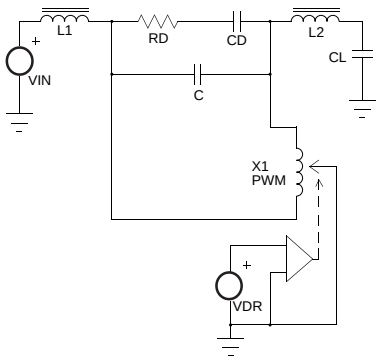


Figure 13, A Cuk regulator with coupled inductors and commutating capacitor damping using the newly developed SPICENET PWM symbol subcircuit model.

A Silicon Controlled Rectifier (SCR) Model

The equivalent SCR subcircuit shown in Figure 14 will be used for the SCR model. SCR's are difficult to model because the typical data sheet does not provide adequate information and the anode gate terminal is not available to generate test data. The approach presented here will focus on making a model that gives reasonable results for dv/dt sensitivity, holding current and storage time. The dv/dt sensitivity is defined as the rate of anode to cathode voltage which will turn the device on without any applied gate current. It varies with gate voltage bias; however, rate sensitive turn on will occur even when the cathode gate is shorted to the cathode. The extra NPN transistor in the model is used to model the lateral base resistance and account for this effect. The 2N6397 data sheet will be used for the sample calculations.

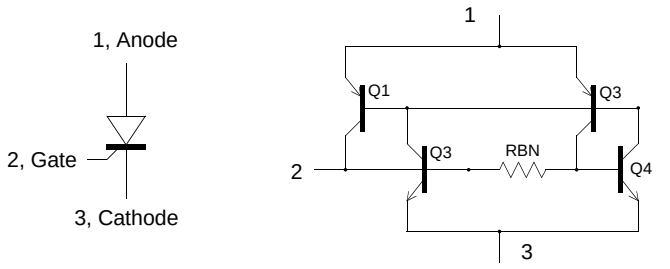


Figure 14, The Intusoft SCR equivalent circuit (Right) and SPICENET symbol, QN6397, (Left).

When the compound Hfe of the NPN and PNP transistors is greater than unity, the SCR will turn on. The 2N6397 data sheet shows the holding current and the DC trigger current to be nearly equal, suggesting the two transistors have about the same Hfe versus current behavior. Hfe will increase at higher currents so that the holding current must be a result of low current Hfe roll off which is modeled by selecting NE and ISE as described by the BJT equations resulting in NE=2 and ISE=4E-9. The value for IS and RBN are initially selected based on the generic power transistor.

The dv/dt specification is 50 v/usec, at 125 Degrees C, where Hfe is typically twice its room temperature value. The trigger current should be one fourth its high temperature value since there is a cascade of two current gains. The SCR should then turn on when the current through the collector-base capacitance is 1.25ma.

$$i = C*dv/dt, \qquad \text{Eq. 7.10}$$

$$Ctotal = Ih/dv/dt = 25PF \qquad \text{Eq. 7.11}$$

This will give a value of about 100PF at zero bias so that the CJE and CJC of the two transistors can be set to 50PF. This capacitance will also affect circuit performance, so independent verification was also be made by laboratory test.

The 40 Ohms resistance connecting the two bases is chosen based on the generic power transistor model. When the gate is shorted, it will be necessary to have an additional 15ma of current through the capacitance, which will increase the dv/dt threshold by a factor of four. Predictions for a typical device at room temperature are then 200 V/USEC open gate and 800 V/USEC shorted gate. In order to obtain proper temperature sensitivity, it is necessary to also set XTB, the forward Beta temperature exponent, to 2.5.

Selecting BF, BR, TF and TR is more difficult. These parameters will describe the dynamic SCR behavior, which is a function of the current distribution when all junctions are forward biased. Experimental evaluation of the simulation parameters shows that the NPN must be slower and have higher gain than the PNP in order for the NPN base emitter to remain forward biased during turn off. If the NPN base emitter turns off first, then a large negative voltage transient is predicted for the gate, a condition that is not observed. Trial simulations were run to determine a reasonable set of gain and transit time parameters. The starting point used the generic power transistor parameters. The final set of parameters is in the SCR.LIB file. Simulations were run to verify DC trigger current, dv/dt, turn on and turn off characteristics. Figure 15 shows the simulation for

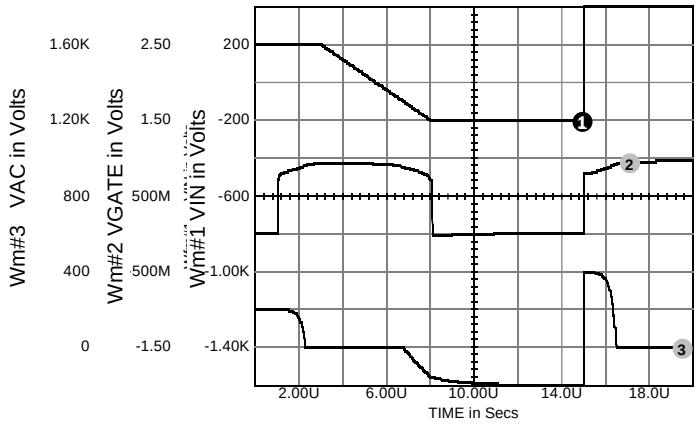


Figure 15, A 2N6397 SCR turn on and turn off response, 125 Deg. C.

turn on and turn off at 125 Degrees Celsius-. where dv/dt triggering is shown.

Special Sources For Power Supply Designers

Included in the Signal.Lib file are several signal sources especially developed to assist the power supply designer. Two sources of special note are the 3 phase generator capable of supplying 3 phase voltages, with or without magnitude and phase error, and a variable phase Sin/Cosine source. [Figures 16a-c].

```
.SUBCKT GEN3 3 7 1 20
* FREQ = {FREQ} AMPLITUDE = {VGEN}
C1 2 20 {1/(6.28319K*FREQ)}
R1 2 20 1E6
I1 20 2 PULSE {VGEN*1U} 0
* MAKES UIC UNNECESSARY
E1 5 20 20 2 1
V1 3 20 SIN 0 {VGEN} {FREQ}
E2 7 20 POLY(2) 5 20 3 20 0 -866.00M -500.00M
E3 1 20 POLY(2) 5 20 3 20 0
+ {(1+.01*MAGERR)*(.866*(1-.5*(.0174533*PHASE)^2)
+ -.5*.0174533*PHASE*(1+.166667*
+ (.0174533*PHASE)^2))}
+ {(1+.01*MAGERR)*(-.5*(1-.5*(.0174533*PHASE)^2)
+ -.866*.0174533*PHASE*(1+.166667*(.0174533*PHASE)^2))}
G1 20 2 20 3 1M
R2 7 0 100MEG
R3 1 0 100MEG
R4 3 0 100MEG
R5 5 0 100MEG
.ENDS
```

3 Phase Generator Subcircuit Listing

The 3 phase generator is made up of an integrator that converts the basic sine source to a cosine source. Summers are then used with varying weighting constants to give the desired output signals. The source allows the user to define the peak amplitude and frequency. Magnitude and phase un-

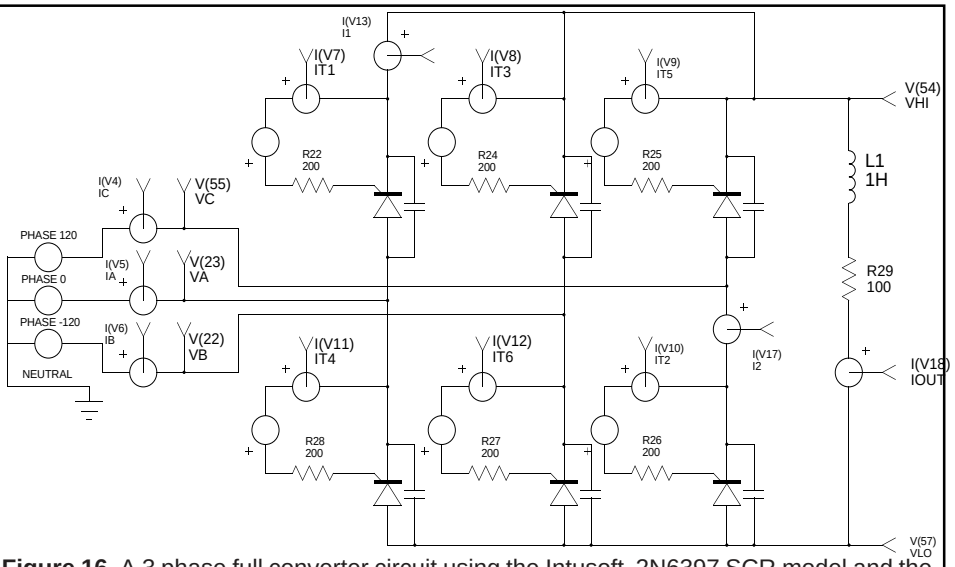


Figure 16, A 3 phase full converter circuit using the Intusoft 2N6397 SCR model and the 3 phase generator source.

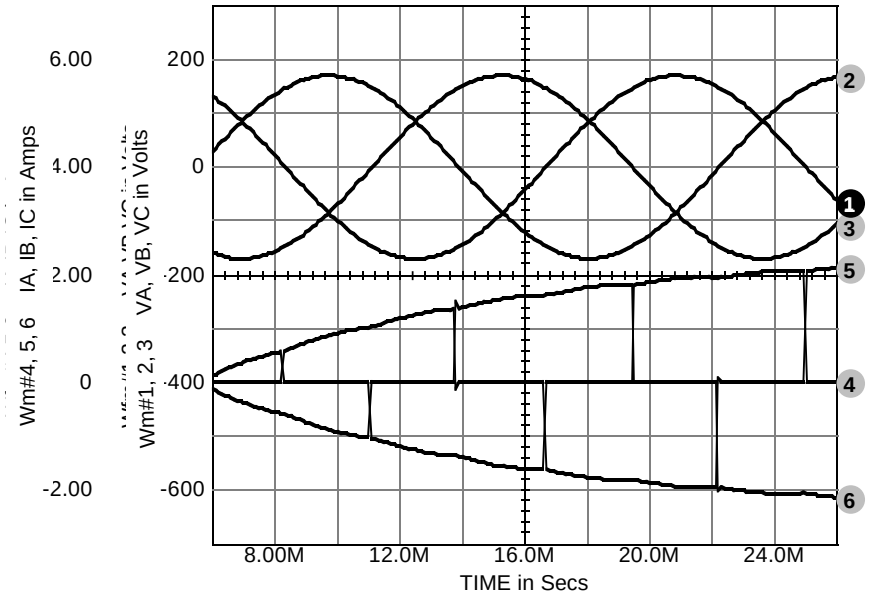


Figure 16a, Current and voltage waveforms for the 3 phase full converter.

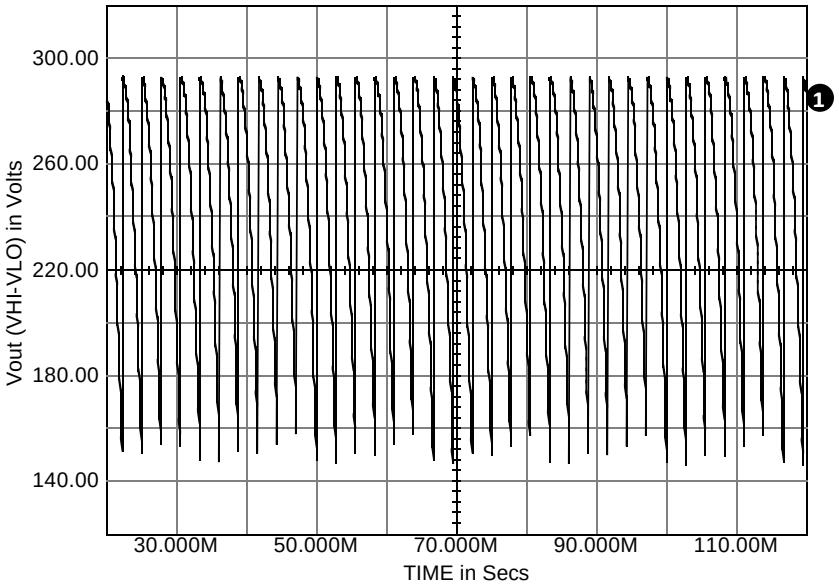


Figure 16b, Output voltage for the 3 phase full converter.

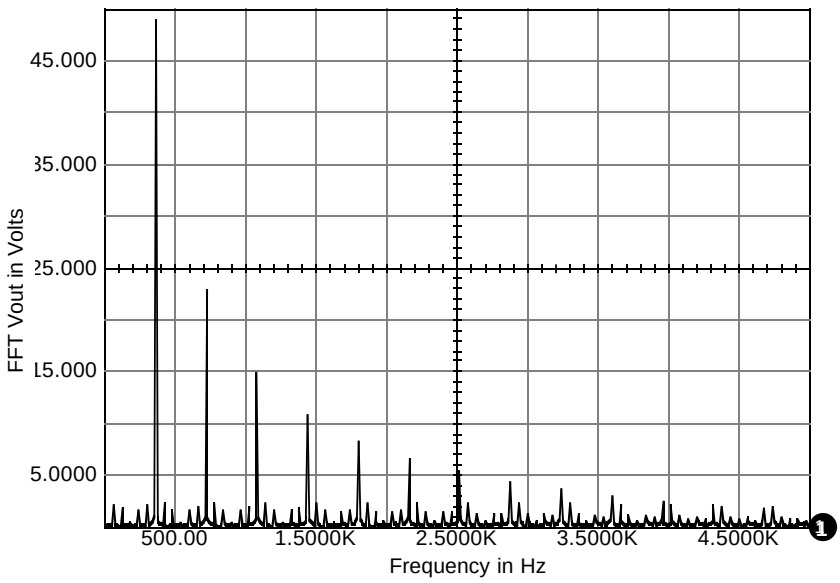


Figure 16c, Frequency spectrum (FFT) of the output voltage for the 3 phase full converter.

balance has been added to the source in order make it possible to evaluate performance parameters that may not be seen in the laboratory.

References

[7-1] SPICE2, A COMPUTER PROGRAM TO SIMULATE SEMICONDUCTOR CIRCUITS
Laurence W. Nagel, Memorandum No. ERL-M520, 9 May 1975, Electronics Research Laboratory, College of Engineering, University of California, Berkeley, CA 94720

[7-2] DESIGN MANUAL FEATURING TAPE WOUND CORES,
Magnetics, Inc., Components Div., Box 391, Butler PA 16001

[7-3] TRANSFORMER MODELING AND DESIGN FOR LEAKAGE CONTROL
Shi Ping Hsu, R.D. Middlebrook and Slobodan Cuk, Powerconversion International, pg. 68, Feb, 1982

[7-4] ADVANCES IN SWITCHED-MODE POWER CONVERSION
Slobodan Cuk and R.D. Middlebrook, vol 2, copyright 1981

[7-5] NEW SIMULATION TECHNIQUES USING SPICE
L.G. Meares, Applied Power Electronics Conference, (c) IEEE, April-May, 1986.

Disk Contents

SM Directory

SM24.CF	Configuration file
SM24.Exe	SpiceMod program
SM24xxx.Txt	Help files
SPICEMOD.BAT	Batch program to call SpiceMod
*.LIB	Sample Model Libraries

MISC-SM Subdirectory

README.DOC	Latest documentation notes
*.CIR	
*.DWG	Test circuit schematics and netlists
*.LNK	
*.CON	

Before Installing SpiceMod

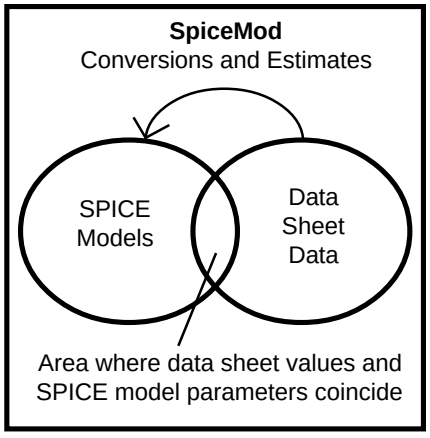
- Check to see that the package contents are complete.
- Make sure you have the correct hardware requirements.
- Hardware Requirements: Any PC or compatible, DOS 3.3-6.x

Chapter 8 - SpiceMod And SPICE Modeling

Why SpiceMod?

SPICE has been an industry standard for analog circuit simulation for over 20 years. In that time, some of the difficult tasks associated with using SPICE such as netlist development, documentation of a design, Monte Carlo analysis, and SPICE data post processing have been solved. With powerful schematic entry, Monte Carlo analysis and waveform post processing tools, ICAP/4 assists the user in getting the most out of SPICE.

However, the most difficult simulation task for the majority of SPICE users has been device modeling. This is due to a number of factors including the lack of device data, the difficulty in determining the important SPICE parameters and sometimes even intimidation. Another major problem is the large number of complex calculations required to convert the data that is generally available into actual model parameters. The figure below describes the problem.



SPICE models are described using a specific set of parameters. The device data available to an engineer is normally in the form of a data sheet. Although laboratory test data can also be used, it too is usually similar to the data presented in the data sheet. SPICE model parameters, on the other hand, do not generally translate directly from data sheet information. As shown above, the area where the two

coincide is small. In order to create a model, a set of mathematical conversions must be produced that will take in data sheet parameters and put out the required set of SPICE model parameters. This is exactly what SpiceMod accomplishes.

What is SpiceMod?

SpiceMod, the SPICE modeling spreadsheet, gives you the power to create an unlimited number of SPICE models for thousands of semiconductors. With SpiceMod, you won't have to curtail or eliminate your simulation activities because you don't have a model, you won't have to spend countless frustrating hours learning the intricacies of SPICE model parameters, and you won't have to make any laboratory measurements. All you need is the manufacturer's data sheet and just a few minutes of your time.

SpiceMod produces accurate models that can be used with any Berkeley SPICE compatible program. File storage is in an ASCII format insuring easy file transfer and editing. Nothing is hidden. All models and subcircuits are available for viewing and editing. And because model development is so streamlined, you can develop minimum, maximum, typical or worst case libraries to cover all of your simulation needs.

SpiceMod is integrated with ICAP/4, Intusoft analog and mixed-signal simulation system. The models and subcircuits created in SpiceMod can be stored in .LIB files. This allows all the models to be immediately used in your SpiceNet schematics and IsSpice circuit simulations.

Rules of Modeling

Even though SpiceMod will be a tremendous help in the creation of SPICE models, there are some guidelines to keep in mind when modeling for SPICE.

- Do not model anything that you don’t absolutely have to. This goes for model functionality, as well as accuracy. It is

a waste of time to try and get an exact model when an approximate one will do. The test circuits contained in the guide will help you evaluate your models. You are encouraged to test your models in simple applications to verify their validity and determine if further refinement is needed.

- Always, remember that modeling is a compromise. Often you will find that it is not possible to exactly match all the data sheet specifications with a single set of model parameters. Prioritize the characteristics that the model must emulate and adjust the model accordingly.

- There is no substitute for knowing what you are doing. To model effectively, you must understand the limitations and features of the model you create and the application the model will be used in. The efficiency and results of your simulations will be determined by the degree to which these factors are known.

Manual Notation

SpiceMod creates two types of SPICE representations for the devices it models. One is a .MODEL statement which is used to model diodes, zener diodes, transistors, JFETS, and MOSFETS. The other is a SPICE subcircuit which is used to model power and Darlington transistors, power MOSFETS, Sidacs, Diacs, SCRs, Triacs and IGBTs. Although the first is usually referred to as a “primitive model”, and the second is referred to as a “subcircuit macro model”, both will frequently be referred to as simply, a “model”, for the sake of convenience. Models and subcircuit models are equal in function, that is, they both represent a physical device. The only difference is how they are implemented in the SPICE netlist description.

What Is ICAP/4?

The term ICAP/4 is mentioned in several places in this user’s guide. For those who are new to Intusoft’s circuit design tools,

ICAP/4 is an integrated set of circuit analysis programs including schematic entry, SPICE simulation, model libraries, and data post processing. If you have an ICAP/4 package, you will be able to run SpiceMod from the ICAP/4 Start menu in Windows 95, 98 or NT,2000.

Installing SpiceMod

To install SpiceMod with ICAP/4 Windows or ICAP/RX

- Insert the ICAP/4 CD-Rom.
- The “Setup” program will start automatically.
- Follow the directions provided by the SpiceMod program.

To install SpiceMod standalone

- Insert the Setup disk into the floppy drive.
- Change to the floppy drive prompt and type “Setup”.
- Follow the directions provided by the Setup program.

Chapter 9 - Quick Start Tutorial

Where To Go From Here

For information on operating SpiceMod, please review the section on Program Operation. The sections on the device types supported, the model effects simulated, the model limitations and how to properly enter data are particularly important. A tutorial guide is also provided to get you started on generating models.

A number of test circuits have been supplied with SpiceMod. They will allow you to test your models and generate waveforms that may be compared to the device's data sheet curves. The circuits are described in the Testing The Models section.

Using the models created by SpiceMod with ICAP/4 is fairly straight forward. A discussion on this topic is included along with information on using SpiceMod models with ICAP/4 and the SpiceNet schematic entry program.

If you have any questions after reviewing the user's guide you should obtain the appropriate references in the "Finding Out More About SPICE Parameters" section.

This tutorial will familiarize you with the basic mechanics of using SpiceMod. After completing this tutorial you will be surprised by the ease with which any model can be created. This section of the tutorial will cover the creation of a SPICE model for a diode. We will learn how to start SpiceMod, enter data sheet parameters, and create a .MODEL statement that

can be used by any SPICE program to simulate a diode. The tutorial will also introduce you to some of the test circuits included with SpiceMod. These test circuits will allow you to verify the integrity of the device models you create. Follow the instructions in **BOLD** to perform the tutorial.

Starting SpiceMod

To run SpiceMod from ICAP/4

- Select SpiceMod from the ICAP_4 submenu in theWindows Start Programs menu or double click the SpiceMod icon in the ICAP_4 Program Group.

To run SpiceMod as a stand alone program

- Change to the SpiceMod directory (Spice8\SM by default).
- Type “SpiceMod” at the DOS prompt.

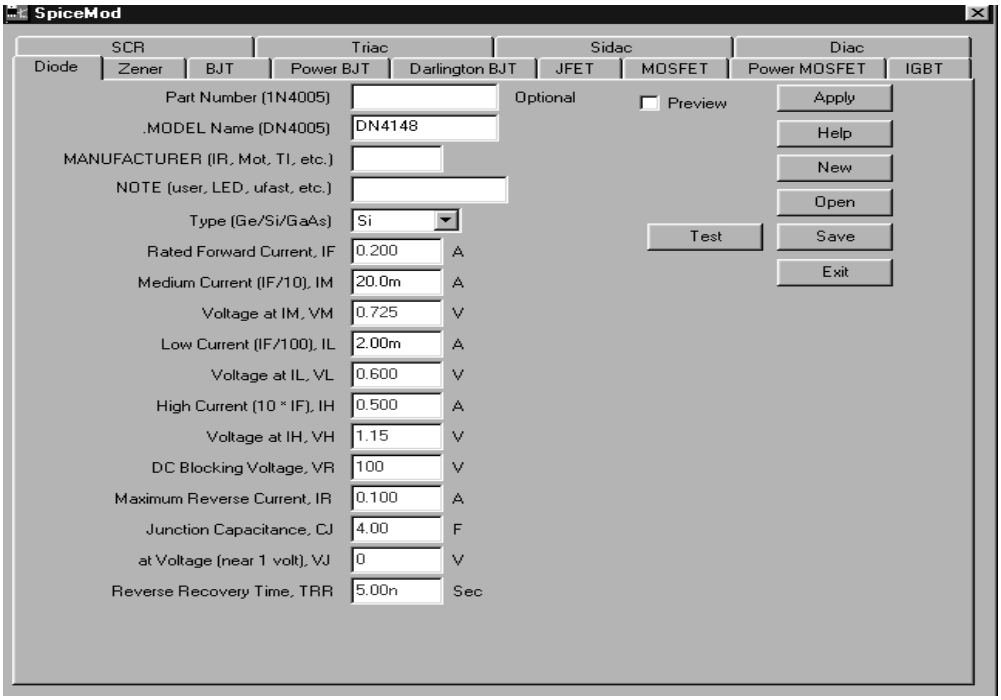
After starting the program you should see the SpiceMod device selection screen.

The Model selection screen displays the various devices that can be modeled with a IsSpice4 .MODEL and .SUBCKT statements.

To choose a menu entry

- Use the arrow keys or press the first letter on the line.

This moves the highlight bar through the available devices that you can model. At the bottom edge of the screen are instructions for help, color selection, library options, and quitting. Now that you are familiar with the SpiceMod environment, lets try some modeling.



Modeling A Diode

The diode for which we will develop a model is the industry standard 1N4148. We will use the data sheets supplied in the Unitrode Corp. data book. Although they are not necessary for the tutorial, it may be helpful to have the 1N4148 diode data sheets available.

SpiceMod contains a different data entry screen for each device type. The data entry screen allows you to input data sheet values and create a SPICE model.

- **Enter data and Press tab to advance to the next field.**

Press the Tab key to move through the various fields displayed on the screen. For pull-down boxes, click the box to select the desired option. The default parameters will be shown initially. As data is entered, the default data sheet parameters will be changed.

Note: Data should be entered in the order that is listed in the data entry screen starting with the first field at the top of the screen and proceeding to the last value. If data is not available, the corresponding entry may be skipped. This will allow SpiceMod to make proper estimates for values that are not entered.

Of course, the more parameters you supply to the spreadsheet the more accurate the final model will be. Most of the parameters the spreadsheet requires are similar to those found on component data sheets.

- **First Enter the Device or Model Name.**

The first step in modeling a diode is to enter the device or model name. To enter data in any field, TAB over the field and type the desired entry. Pressing the TAB is the equivalent of pressing APPLY to accept the data.

Generally, you may give a model any name, however, it should not be more than sixteen characters in length and should start with an alphabetic character. The model name is used to find the model in the model library. Start with a letter and use only eight characters to be compatible with earlier SPICE versions. For diodes, it is a good idea to start the model name with the letter “D”.

Next, we can select the type of semiconductor material, either **Ge**rmanium, **Si**licon, or **GaAs.** Since the 1N4148 is a silicon diode, we can leave the material field at its default value of “Si”.

The next parameter to be entered is the rated current. Rated current for a device can be found in some data book selector guides; some data sheets display it as a device feature. If either of these are not available, use the average output current which is usually found in the maximum ratings section of the data sheet. Do not use the surge current value.

- **Move to the Rated Forward Current field by pressing the Tab key. Type “0.2” in the IF field.**

Notice that the entered values are now highlighted. Also, note that some of the values changed in both the interface and the SPICE model. SpiceMod updates its estimates of the data sheet and SPICE model parameters after you enter each value.

The next six parameters, IM, VM, IL, VL, IH, and VH, can be entered provided that the data sheet has either a forward voltage and current curve or a table containing voltage and current values taken in the forward bias mode. If no data is entered these parameters will be estimated from the rated current entry. We will be using the 25° C curve to extract the data points needed by the spreadsheet. In fact, you should normally create all models using data taken at room temperature since SPICE will normally handle temperature variations for the models developed by SpiceMod.

Check the default units before entering any parameter values.

We will skip entering IM and IL since the estimated values appear on the data sheet curve and enter the values for VM and VL. From the IV curve, VM is equal to 0.725, and VL is equal to 0.6.

- **Type “0.725” in the VM field.**

- **Type “0.60” in the VL field.**

Now we will enter values for IH and VH. From the curve we will use 500mA for IH and 1.15 Volts for VH.

- **Type “0.5” in the IH field.**

- **Type “1.15” in the VH field.**

That completes the modeling of the 1N4148 diode behavior in the forward region. The next two parameters requested are the reverse breakdown voltage (VZ) and the associated current (IZ). Turning again to the data sheet; the reverse breakdown voltage can most often be found in the Absolute Maximums section. The current at breakdown is sometimes listed, just after or as part of, the reverse breakdown voltage specification. Sometimes, a reverse voltage versus current curve is given

from which the spreadsheet parameters can be found. For our model, we will use an absolute maximum rating for the reverse voltage and determine the reverse current from a curve. From the data sheet, VZ=100 Volts and IZ=0.1µA.

- **Type “100” in the VR field.**

- **Type “0.1” in the IR field.**

Notice that the IZ parameter has the default units of microamps. Had we entered 0.1E-6 for IZ, the spreadsheet would have assumed a value of 100fA. Be aware of the units just to the right of the entered value for all spreadsheet entries. They are always active and will be used in the calculation of the SPICE model parameter values.

That defines all of the DC behavior of the diode. We could stop here and the spreadsheet would estimate the remaining parameters CJ, VJ, and TRR, but it is best to input as much data as is available. Because the 1N4148 is a switching type of diode, entry of the final charge storage and reverse recovery values are critical to obtaining the proper transient behavior.

The next two parameters, CJ, and the voltage for the VJ, are used to determine the diode capacitance parameter, CJO. Referring to the data sheet, CJ, or junction capacitance, is sometimes listed in a table. Some data sheets provide a curve which shows the capacitance behavior over a wide range of reverse voltage. The data sheet we are using provides the data in a table. From the data sheet, CJ=4.0pF at a VJ of 0 (zero) volts. It is best to use the capacitance at zero applied voltage since this will correspond exactly to the CJO value. Otherwise, the combination of CJ and VJ will be used to determine the CJO value.

- **Type “4.0” in the CJ field.**

- **Type “0” in the VJ field.**

The last parameter to enter into the spreadsheet is the reverse recovery time, TRR. This parameter defines the time it takes to

switch the diode from completely on to completely off. Most data sheets list the parameter in a table. The data must be taken at the point where the forward current is equal to the reverse current or IF=IR. Turning to our data sheet, the reverse recovery data is given in a table as TRR=5ns.

- **Type “5n” in the TRR field.**

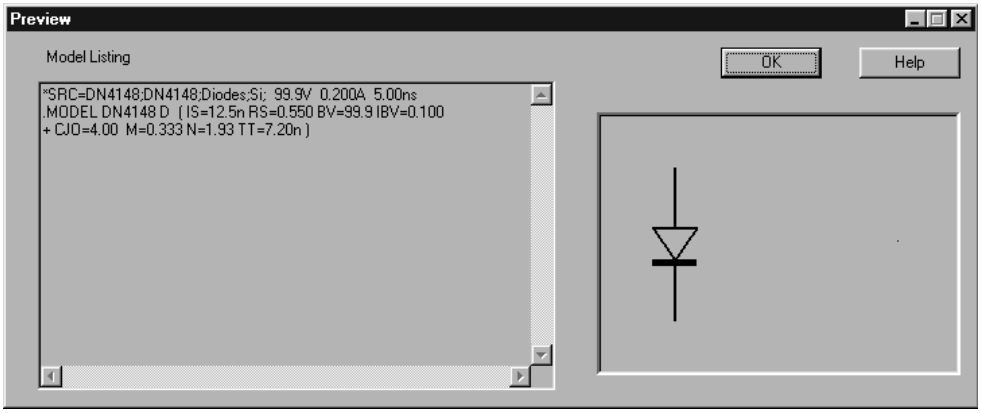
Notice again that the default units could have caused an erroneous entry if only the number “5” was entered. Please be aware of the default units of the interface. We are now finished generating the model.

In order to view the completed model listing, check the preview box. The completed model is shown for comparison.

- **Check PREVIEW to view the completed model listing.**

Clicking preview causes SpiceMod to display the resulting .MODEL statement. You can actually see the model parameters update as you enter data in each field.

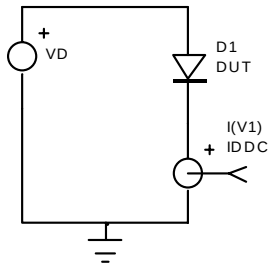
- **Click SAVE to save the model listing.**
- **Click TEST to open Library Manager.** (Available to users ofTest Designer, ICAP/4 Professional, Power Supply Designer, and Magnetics Designer only).
- **You can exit SpiceMod by pressing Exit.**



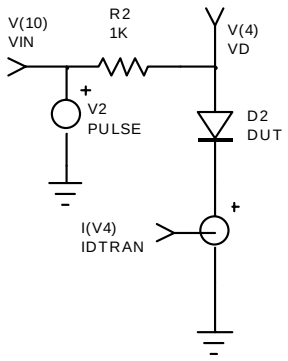
Testing The Diode Model

Now that the model is complete, we can verify the performance. To test the 1N4148 diode we have just created, we will use the SPICE test circuit called DIODETST.CIR. This test circuit has two parts and performs two tests; diode forward current vs. voltage and reverse recovery time. The schematic diagrams for the test circuits are shown below. The SPICE netlists and instructions for these circuits can be found in the Testing The Models section later in this guide.

FORWARD CURRENT TEST CIRCUIT



REVERSE RECOVERY TIME TEST CIRCUIT



Initially, the test circuit is set up in a default configuration suitable for most diodes. The type of diode and its ratings will dictate if you need to modify the SPICE voltage or control statements.

You must update the SpiceNet database before a model can be tested.

Note For Library Manager users: With Library Manager, you can preview and test your circuit and your model listing will be updated automatically.

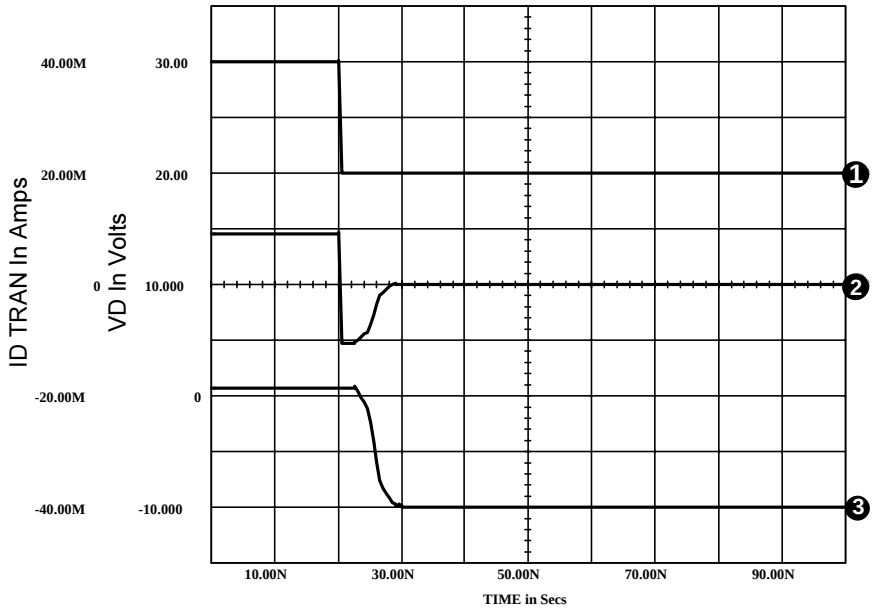
Note For other ICAP/4 users: If you do not have Library Manager, you must first delete the DUT device and insert the device you want to simulate, in this case, the 1N4148. To do this you MUST first get the model into the SpiceNet database.

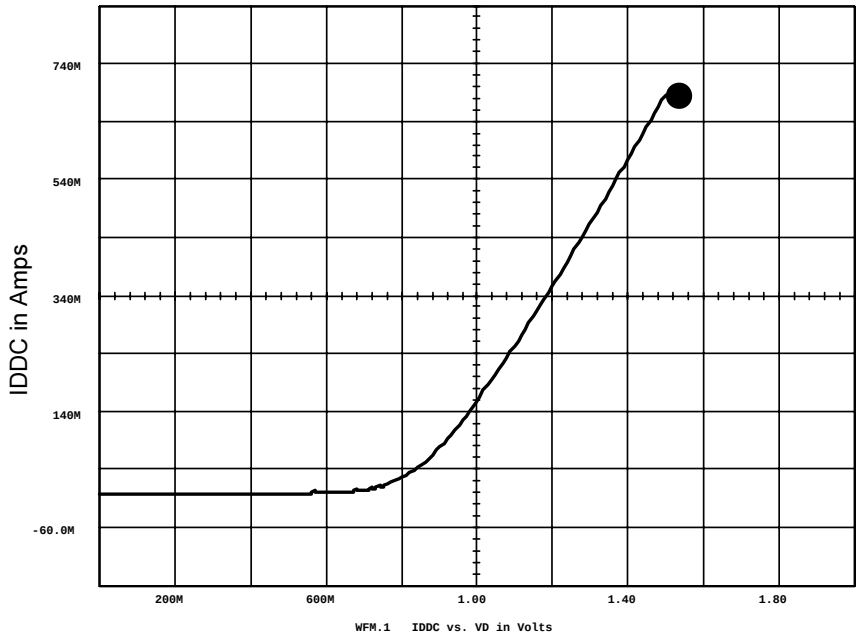
This is accomplished by putting the library file containing the model into the SPICE8\PR directory, if it is not already there.

Then you must update the SpiceNet database by selecting Update Database from ViewDraw's File menu. See the SpiceNet on-line help for more information.

If you are using any another SPICE program, you will have to retrieve the .MODEL statement from the model library file where it was saved and place it into the DIODETST.CIR netlist using a text editor before a SPICE simulation can be run.

The DIODETST.CIR should produce the results shown below.





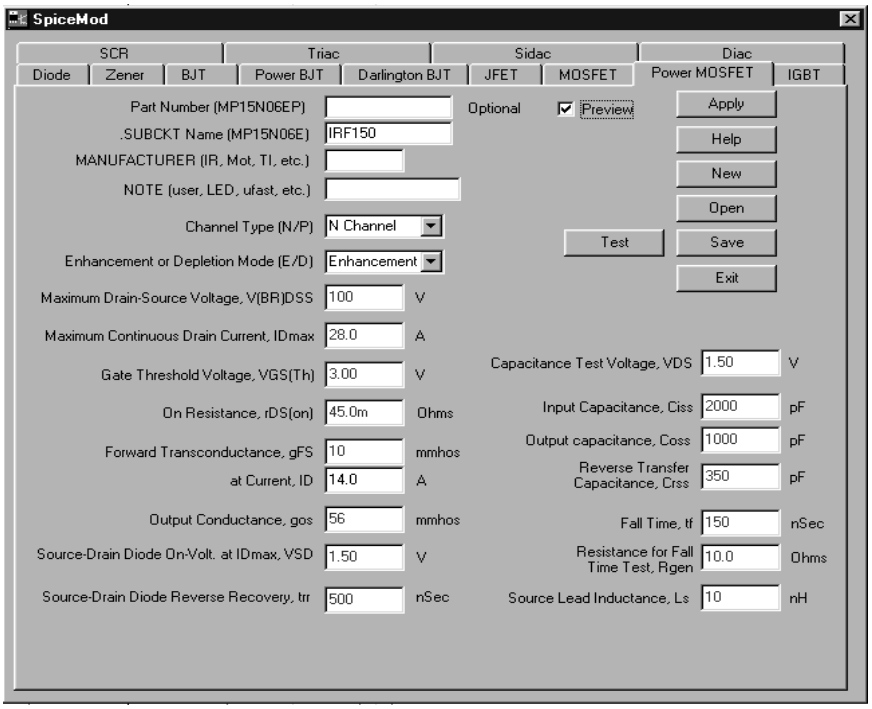
Diode Current vs. Voltage using DC Analysis

A complete description of all the test circuits included with SpiceMod and their use can be found in the Testing The Models section. In this section we have successfully modeled the 1N4148 diode. In the next section we will develop a model for a power MOSFET.

Modeling A Power MOSFET

Modeling a power MOSFET, which uses a SPICE subcircuit representation, is much like modeling a diode. The power MOSFET subcircuit consists of more than just the basic SPICE primitive MOSFET model. It also contains other circuit elements including diodes, resistors, capacitors, and dependent sources. SpiceMod uses a subcircuit rather than a single MOSFET element because the basic MOSFET is not sufficient to model all the important effects exhibited by power MOSFET devices.

In this section we will be modeling an IRF150 N-channel MOSFET using the Power MOSFET subcircuit. The IRF150 data sheet is listed in the International Rectifier HEXFET Designers Manual. This section assumes you have completed the diode modeling portion of the tutorial.



Modeling the IRF150

- **Begin by starting SpiceMod and selecting the Power MOSFET tab.**
- **Type the .SUBCKT name “IRF150”.**
- **Skip over the channel type and enhancement or depletion mode entries since the default entries are valid.**

The next entry, for the maximum drain-source voltage, is found on the data sheet in the absolute maximums table. For this device VDSS = 100 Volts.

- **Enter 100 into the V(BR)DSS field.**

The next entry can also be found in the absolute maximums table. The maximum continuous drain current for this device is 28 Amps.

- **Enter 28 into the IDmax field.**

As you can see, the power MOSFET model has many more elements than the simple primitive diode model.

The next parameter is the threshold voltage which is normally listed in the electrical characteristics portion of the data sheet. For this device Vgs(th) = 2 to 4 Volts.

- **Enter 3 Volts into the VGS(th) field.**

When a data sheet gives the Min and Max values for a parameter, it is customary to use an average value for a typical model. This value may be refined later using feedback from the test circuits. The remaining parameters are listed next in the order that they appear in the interface.

- **Enter these parameters into the interface.**

Rdson = .045Ω	**On resistance**
gfs = 10 mohs	**Forward transconductance**
Ciss = 2000 pF	**Input capacitance**
Coss = 1000 pF	**Output capacitance**
Crss = 350 pF	**Reverse transfer capacitance**
tf = .15 µs	**Fall time**
Rgen = 10 Ω	**Generator resistance for fall time test**
Vsd = 1.5 Volts	**Diode forward voltage**
trr = 500 ns	**Reverse recovery time**
Ls = 10 nH	**Source lead inductance for a TO-3 package**

- **Press preview to view the created model.**

- **Press save to store the created model.**

The power MOSFET subcircuit can now be tested using the test circuits listed in the Testing MOSFETS section.
This completes the Quick Start Tutorial. From here you should review the Program Operation and Program Notes sections in order to resolve any technical questions.

This section describes the operation of SpiceMod, the model capabilities and limitations, the procedures surrounding data entry, and the instructions on model storage/library maintenance.

Quitting SpiceMod

To quit SpiceMod

- Press the Exit key.

To quit SpiceMod if you are in one of the data entry screens

- Press the Esc key. This will terminate the data entry process. You will be asked if you want to save the current model.

- Either save the model by pressing enter, or discard the model by pressing “N” and enter. If you press “N”, you will be returned to the main device selection screen.

- Press the Esc key, followed by the Enter key to exit the program.

Chapter 10 - Program Operation

This section describes the operation of SpiceMod, the model capabilities and limitations, the procedures surrounding data entry and the instructions on model storage/library maintenance.

Starting SpiceMod

To start SpiceMod

- Double click on the SpiceMod icon in the ICAP_4 program group.
- You may also use the Start menu. Navigate to the Programs ICAP_4 submenu and select SpiceMod.

A batch file, SpiceMod.Bat, will run and call the SpiceMod executable program.

Device Types Supported

The device types SpiceMod can create SPICE models for are listed below. SpiceMod can create models for devices using any component vendor's data sheets.

Diodes (Silicon, Germanium, GaAs, Schottky)**, Zeners**
Typical applications: PN, computer, switching, rectifier, diode bridge, zener, avalanche regulator, voltage reference, transient suppressors, varactors; low, medium, and high power, any frequency range.

Transistors - Silicon, Germanium, NPN, and PNP
Typical applications: small signal, switching, amplifier, choppers, telecom, low and medium (40-200 Volts, 5-50 Amps) power, frequency range below RF.

Power Transistors - Silicon, Germanium, NPN, and PNP
Typical applications: switching, regulator, converter, inverter, amplifier, automotive; medium and high power, frequency range below RF.

Darlington Transistors - Silicon, Germanium, NPN, and PNP
Typical applications: high gain, high input impedance, switching, regulator, amplifier, automotive; low, medium, and high power, frequency range below RF.

JFETS - N / P Channel, Depletion and Enhancement mode
Typical applications: small signal, switching, choppers, amplifier, voltage controlled resistors, current limiting; low, medium, and high (below RF), low noise, low leakage.

MOSFETS - NMOS, PMOS, Depletion, Enhancement
Typical applications: small signal, switching, choppers, amplifier, telecom, dual-gate Mosfets, Photo-Mos, CMOS logic; low and medium power, frequency range below RF.

Power MOSFETS - NMOS, PMOS, Depletion, Enhancement Typical applications: switching, amplifier, automotive; medium and high power, frequency range below RF.

SCRs/Thyristors/GTOs/Triacs/Alternistors/Diacs/Sidacs Typical applications: power rectification, crowbar circuits, motor control circuits, opto-couplers, relay and lamp driver circuits. Low to high reverse blocking voltage, moderate to high forward current capability.

IGBTs - N/P channel with or without diode. Typical applications: uninterruptable power supplies, motor control circuits, general switching and high voltage switch mode power converters, frequency range from DC to 100kHz.

Model Effects Simulated

Listed below are some of the major characteristics that the SpiceMod models will exhibit when simulated using ICAP/4.

Diodes, Zeners: DC characterization, Voltage vs. Current response, transient switching effects, capacitive effects, forward voltage temperature variations, reverse conduction, charge storage, power dissipation.

Transistors: DC characterization, transient switching, capacitive effects, hFE vs. IC vs. temperature, early effects, VBE temperature variations, charge storage, power dissipation.

Power Transistors: DC characterization, transient switching effects, capacitive effects, VBE temperature variations, transistor turn-on and turn-off.

Darlington Transistors: DC characterization, transient switching effects, capacitive effects, VBE temperature variations, transistor turn-on and turn-off.

JFETS: DC characterization, transient switching effects, capacitive effects, temperature variations, power dissipation.

MOSFETS: DC characterization, transient switching effects, capacitive effects, temperature variations, power dissipation, Level 1 model only.

Power MOSFETS: DC characterization, transient switching effects including asymmetrical turn-on and turn-off times, gate charge curves (dual slope drain voltage waveform with dynamic Vsat behavior), inductive switching effects, all capacitive effects including nonlinear gate to drain capacitance and proper Crss, Ciss, and Coss modeling, temperature, parasitic source inductance, power dissipation, Level 1 or Level 3 model depending on voltage rating.

SCRs, Triacs, Diacs & Sidacs: DC, switching, dV/dt, holding current, gate trigger current and voltage, forward and reverse breakdown voltages and leakage current.

IGBTs: Switching loses, on-voltage, turn-on/turn-off delay, rise time/fall tail, active output impedance, nonlinear capacitance effects, forward/reverse breakdown, and collector family curves including mobility modulation.

Models vs. Subcircuits

Some common power and RF semiconductors cannot be modeled with the standard SPICE .MODEL statement. This is because the built-in SPICE model for BJTs and MOSFETs are not capable of representing critical large-signal characteristics including various dynamic parameters and package parasitics. A subcircuit approach, using several elements, is required in order to accurately reproduce the device's behavior and important higher order characteristics. For example, nonlinear gate-drain capacitance, substrate diode, and lead inductance can not be modeled for a power MOSFET device using only the standard SPICE MOSFET model.

Sometimes, it is possible to alter the standard model parameters in such a way as to make the device exhibit a desired effect. However, using SPICE parameters out of bounds to force fit the standard SPICE model to the actual device behavior is not recommended and will usually result in improper simulation results. This is why SpiceMod uses subcircuit representations for power and Darlington transistors, power MOSFETS, SCRs, Triacs, Diacs, Sidacs, and IGBTs.

Note: whether you use the .MODEL or subcircuit representation created by SpiceMod, both will be compatible with virtually all SPICE simulators.

Model Limitations

There are a number of important limitations to the models developed by SpiceMod. Some of these effects are due to the inherent limitations in SPICE. Others are due to approximations necessitated by limited data sheet data. The models are designed to be consistent with current semiconductor technology and avoid common errors made by those unfamiliar with SPICE model design.

Diode: Reverse breakdown temperature coefficient, forward recovery time, thermal feedback that causes junction temperature to change as a function of power dissipation, no alteration of the default built-in potential/grading coefficient. Forward characteristics and voltage temperature characteristics in the zener diode model.

Transistor, Gummel-Poon Model: No A.C. current crowding, VAF (Early effects) constant, ohmic resistances have no temperature dependence, neither forward nor reverse bias second breakdown is modeled, quasi-saturation not modeled, no thermal self heating or crosstalk, and inverted operation parameters (IKR, ISC) are not modeled (Since data book information is usually not available for these parameters. These parameters come into play only when the collector-base junction is forward biased.)

Power transistor: The model does not simulate the more complex effects (dual slope turn off time, quasi-saturation) of nonlinear base and collector resistance.

JFET: No noise parameters.

MOSFET: Level 1 model (Shichman-Hodges) only, not for devices with very small geometries (<2µm).

Power MOSFET: No drain inductance (but some can easily be added to the subcircuit model)

SCR, Triac, Diac, Sidac: Inherent limitations of the BJT model such as temperature dependence of ohmic resistances.

IGBT: The inherent limitations found in the BJT and MOSFET models are passed on to the IGBT. Drain inductance, particularly important in fast switching applications, and temperature effects are not modeled but can easily be added.

In general, the SPICE parameters for noise (AF, KF) are not generated by SpiceMod and the junction potential/junction grading coefficient (VJ, M) parameters are not modified. If the proper data is available, these parameters can be calculated. Please see the section on "Adding More SPICE Parameters" for information on how to add these model parameters to the models created in SpiceMod.

Selecting The Device Type and Entering Data

SpiceMod contains a different tab for each device type. The device tab allows you to input data sheet values and create a SPICE model. See the BJT entry screen shown.

To enter data

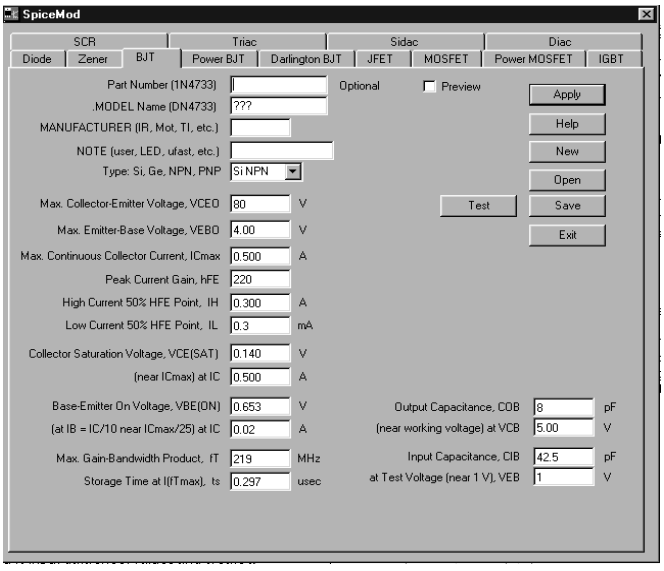
- Click to select the device type you want. Press the TAB arrows to move the highlight bar to the field you wish to change. As the bar is moved, each value will be shown in inverse video. Any default or previously entered value can

be changed by simply typing the new entry when the value is shown in inverse video. Select F4 to change all parameters back to the default value. Select F3 to change one individual parameter back to the default value.

Note: Data should be entered in the order that is listed in the data entry screen starting with the first field at the top of the screen and proceeding to the last value. If data is not available, the corresponding entry may be skipped. This will allow SpiceMod to make proper estimates for values that are not entered.

Data Entry Scaling

All of the data entry fields have been scaled to allow the easiest entry and translation of common data sheet parameters. The scaling factors and units listed to the right of the data entry field are always in operation. The data fields' scaling values should have the same scaling as the values contained in most manufacturers' data sheets. If this is the case, entering the equivalent data sheet parameter is trivial and the exact data sheet value may be entered into the field. If this is not the case, data may be entered using numbers or engineering notation along with the



scaling value, if any, in order to achieve the desired parameter value.

For example, if the data sheet value for the diode reverse recovery time was in seconds, the value (5) could be entered directly into the “trr” data field. If the data sheet value for the reverse recovery time was in nanoseconds, 5 n should be entered, or in microseconds 5 u should be entered.

Caution: Entering one or more data sheet values that make no physical or logical sense will cause SpiceMod to produce an inaccurate SPICE model or cause SpiceMod to declare an illegal entry if the value is abnormally out of bounds.

Special Data Fields

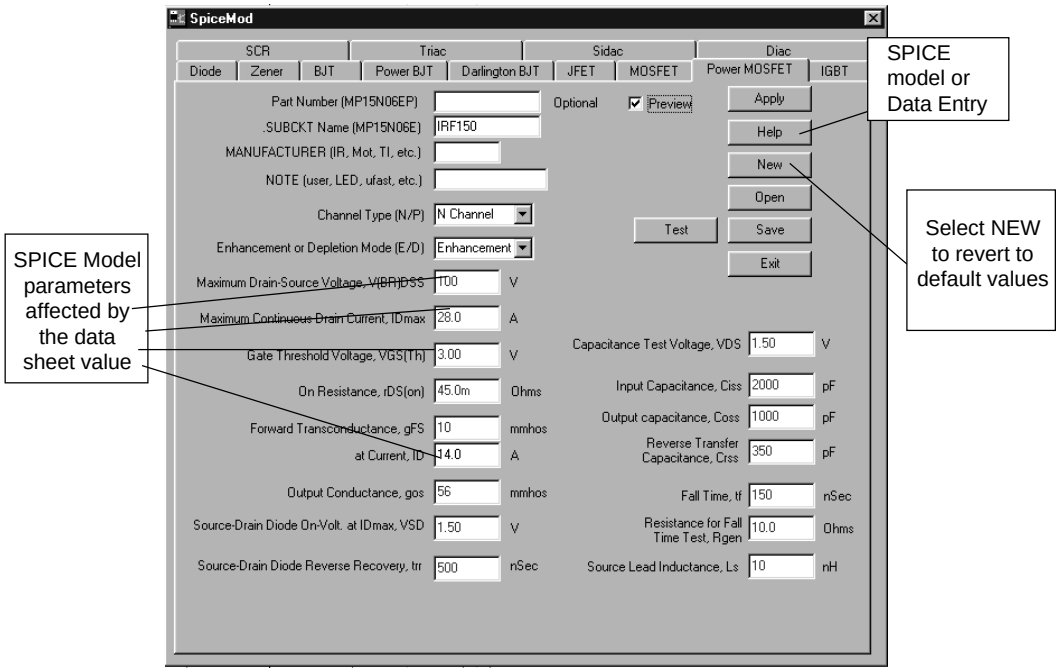
.MODEL Field - This field is used to hold the model or subcircuit name. All SPICE model and subcircuit names should begin with an alphabetic character. All entered data will be automatically converted to upper case when the enter key is pressed.

Type Field - Each device type can be further characterized using the type field. Diodes, transistors, power transistors, and Darlington transistors using the material (Silicon, Germanium, or GaAs) and the polarity (NPN, PNP) can be specified. JFETS, MOSFETS, and power MOSFET models allow the channel type (N/P) and the mode (Enhancement or Depletion) to be selected. IGBTs allow selection of either P or N channel types.

To select the entry for the Type, Channel, or Model field:

- Move to the data field and enter one of the names listed to the left in parentheses. Abbreviations for some of the names may be available (N for NPN, P for PNP, Ga for GaAs, D for Depletion, etc.). Some other fields (Darlington Transistor) may require a “Y” or “N” response.

Other Data Entry Fields - All other fields require some sort of numeric input. Entries beginning with an alphabetic character will not be accepted.



Resetting Altered Data Fields

Click the NEW button to reset each data field to its previous value.

All user entered parameters are shown in blue indicating a change from the default value. To reset all altered data fields to their default values, press NEW or the F4 key. To reset a single data field to its default value, press the F3 key.

SpiceMod Estimates

One of SpiceMod's most important features is its ability to estimate the data sheet parameters that you are not able to enter. The data sheet estimates are based on the data that is entered. As more data is entered, the estimates will be refined. The goal, of course, is to complete the entire data entry screen and not allow SpiceMod to make any estimates. Entering data in all the available fields will allow SpiceMod to create the most accurate model possible.

The interrelationships between the data sheet parameters and the model parameters are quite complex. It is not always clear how a given data sheet value will affect one or more of the SPICE model parameter values. The SPICE model parameters shown to the right of most data fields will give an indication of which model parameters will be affected by the particular data sheet value.

Normally, data field values are dependent on each other. When one value is entered, several other fields and the resulting SPICE model may be changed. For instance, changing the Rated Current, will cause virtually all the other data fields to be changed. However, any user entered values will override these defaults or estimates. Data fields will no longer be estimated or adjusted based on alterations to other fields once a value has been manually entered.

Entering The Right Data

SpiceMod is quite sensitive to the input data. Entering a wrong value, whether typed incorrectly or with the wrong scaling units, can cause the resulting model behavior to be slightly off or completely inaccurate. Under all circumstances, you should check and double check the data values that you enter carefully.

Tolerances on data sheet values vary widely. The data curves and values that are given will usually be maximum, minimum, or typical. If, for example, typical values are input, the curves that are generated when the model is tested should match typical data sheet curves fairly closely. However, some data sheet parameters, which greatly affect a model's performance, can have a very wide range of specification. Sometimes 400 to 500% tolerances can be found on critical parameters such as threshold, capacitance, gain, and so forth. Other times only a maximum or minimum value will be available and a guess of the value will have to be made depending on the type of model (maximum, minimum, typical, or worst case) you are trying to create.

Therefore, do not be surprised if the model does not exactly match the data sheet curves when it is tested. Part of the discrepancy may be due to your estimate of the data sheet values. Part may be due to the SpiceMod estimation of data sheet parameters or its calculation of SPICE model parameters. Even the inherent limitations of SPICE can adversely affect the model's performance. The most important point is to realize which differences are critical to your application and then try to minimize them.

Getting Help

To get help on general topics or an overview of SpiceMod:

- PressHELP key. The on-line help screen will be displayed.

Reading Data Sheet Values

Creation of a model must be done with a consistent set of parameters, for example the temperature at which the data sheet values are taken should remain constant throughout. Generally speaking, data sheet values should be taken from data at 25 degrees C. ICAP/4 will handle most of the temperature variations when the temperature is changed in the simulation.

Minimum Data Requirements

The minimum data sheet values that are required to create a model are listed. The small number of data sheet parameters may seem to be insufficient for generating even a basic model. However, before creating a model SpiceMod will first estimate the unknown data sheet parameters, and then, calculate the SPICE model parameters. Therefore, even if only the minimum set of data is entered, no dynamic SPICE parameters will be left at their default values, thus producing a model with reasonable DC, AC, and transient behavior.

Minimum Data Requirements For A Model

Diodes	Rated Current
Zeners	Zener Voltage and Power Rating
Transistors	Maximum Collector-Emitter Voltage and Maximum Collector Current
Power Transistors	Maximum Collector-Emitter Voltage and Maximum Collector Current
Darlington Transistors	Maximum Collector-Emitter Voltage and Maximum Collector Current
JFETs	Gate-Source Breakdown Voltage, Maximum Drain Current, Gate-Source Cut-off Voltage
MOSFETs and Power MOSFETs	Maximum Drain-Source Voltage, Maximum Drain Current, and Gate Threshold Voltage
SCRs	Peak Repetitive Forward and Reverse Blocking Voltage, Gate to Cathode Reverse Voltage, RMS Forward Current
Triacs	On-state current, Repetitive Peak Off-state Voltage
Diacs/Sidacs	Breakover Voltage, Breakover Current
IGBTs	Collector to Emitter Breakdown voltage, Max. Collector Current, Gate Threshold Voltage

Viewing Models And Subcircuits

The diode, BJT, JFET, and MOSFET are modeled with a .MODEL statement. The Power BJT, Darlington transistor, SCR, Triac, Diac, Sidac, IGBT and power MOSFET devices are modeled with the SPICE .SUBCKT statement.

To view the SPICE netlist for these devices, press the PREVIEW key. Pressing the tab key will move your cursor to the help/netlist screen so that you can scroll through it.

The .MODEL statement or subcircuit listing shown on the screen is exactly what will be saved in a file when you exit the data entry screen and save the results.

Saving And Replacing A Model

To save a model, after you are satisfied with the data entered into the screen, press the SAVE key. You will then be prompted to save the newly generated model or subcircuit. The model will be saved as a *.sm file. A .sm file is text file which lists all of your parameters. Your model will be saved in the \spice8\sm\MODELS subdirectory and within the file folder you select.
If the model or subcircuit is not found in the library, your new model will be saved. If the model/subcircuit name is found, you will be given the opportunity to replace the stored model with your newly created model.

As a user ofTest Designer, ICAP/4 Professional, Power Supply Designer or Magnetics Designer, you will have the option of saving your model in Library Manager, which comes with these programs. With Library Manager,a .lib file is added automatically to your library. A .lib file is the actual netlist that you see in the PREVIEW menu.

If you don't have Library Manager, when you press SAVE to create a .sm and a .lib file, move the .lib file to the \spice8\pr subdirectory and run MAKEDB to update your netlist files.

Any number of models or subcircuits may be placed in a particular file. By placing several models and/or subcircuits into one file, you can create libraries of devices. You may choose to group the elements in a library using any characteristics you choose.

If the model or subcircuit is not found in the library, your new model will be saved. If the model/subcircuit name is found, you will be given the opportunity to replace the stored model with your newly created model.

The models and subcircuits will be placed in the file, each separated by a row of asterisks. This is the exact format required by the ICAP/4 program and is the same format used by other ICAP/4 .LIB model library files. If you are using ICAP/4, the files you create will be ready to use without any modifications.

Editing And Viewing Stored Model Files

Library Manager brings up a list of all the models in a library and its status compared to the one archived. The user can see the model netlist and the difference between the current model and archived model. The user has the option of either deleting the current model or replacing the current model with the archived model.

An existing library can be selected or a new one can be created.

Chapter 11 - Program Notes

Getting The Most Out Of SpiceMod

For many circuit simulations only an approximate model is needed. This does not mean that a SPICE model can be used without changing the defaults on critical dynamic parameters. It means that a model that approximates the general behavior of the device, with realistic performance, but with an overall less degree of accuracy, can be used. This is where SpiceMod can be of tremendous assistance.

As the “Minimum Data Requirements” section points out, models can generally be created with only the maximum device ratings for voltage and current. SpiceMod will then make estimates for the rest of the data sheet values. The estimated values will be used to create a SPICE model. This estimation capability is extremely important because it will always provide data from which a model can be generated. The resulting model will allow a realistic simulation, including many important higher order effects.

Maximum, Minimum, Typical, And Worst Case Models

SpiceMod is setup to allow designers to make a number of models of a similar type quickly and easily. After creating and saving a model, you will notice that if you re-enter the same device data entry screen, all of your previously entered data will have been saved. Variations of the device model can now be made with great ease. This feature allows easy development of maximum, minimum, typical and worst case models simply by varying the desired parameters. All the other parameters will remain as before.

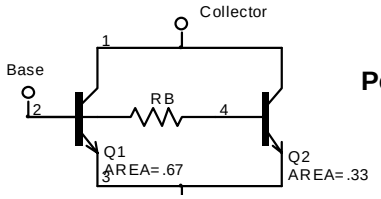
What-If Models

SpiceMod is also capable of creating models for devices that do not actually exist. For example, if the designer does not know the exact component, but does have the electrical specifica-

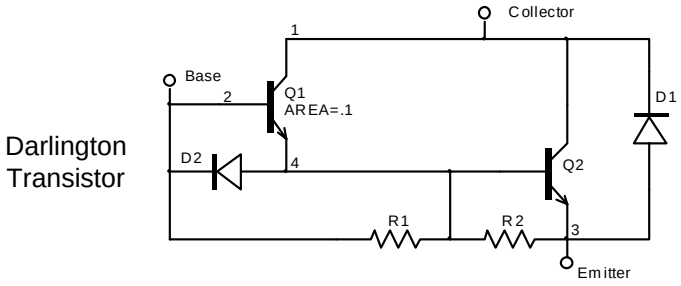
tions for the component, a model could be developed. This would allow the simulation to be performed immediately, and the actual search for a real device can be performed at a later time.

Subcircuit Configurations

SpiceMod uses subcircuit representations for power transistors, Darlington transistors, power MOSFET, SCR, Triac, Diac, Sidac, and IGBT devices. The configurations of some of these subcircuits are shown next. The diodes and resistors shown in the Darlington transistor subcircuit are optional.

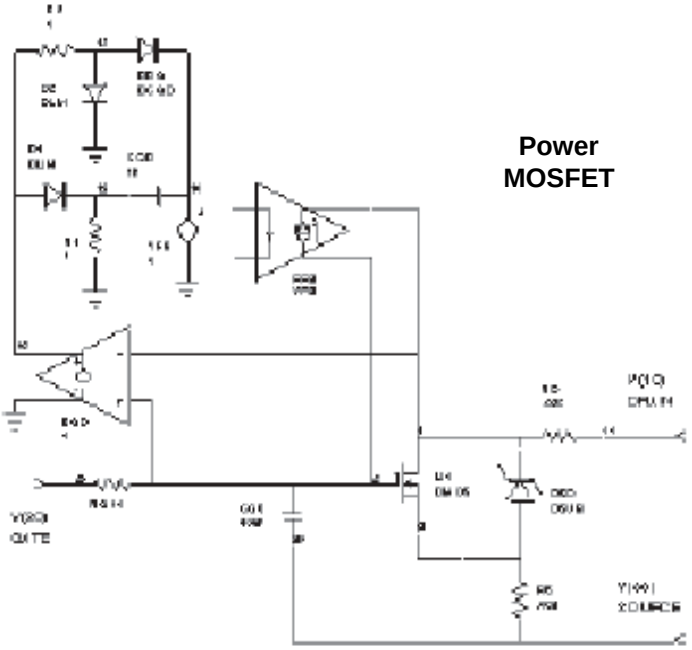


Power Transistor

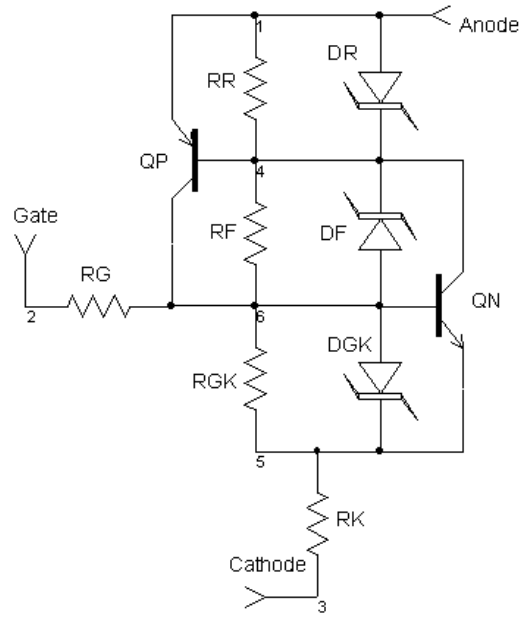


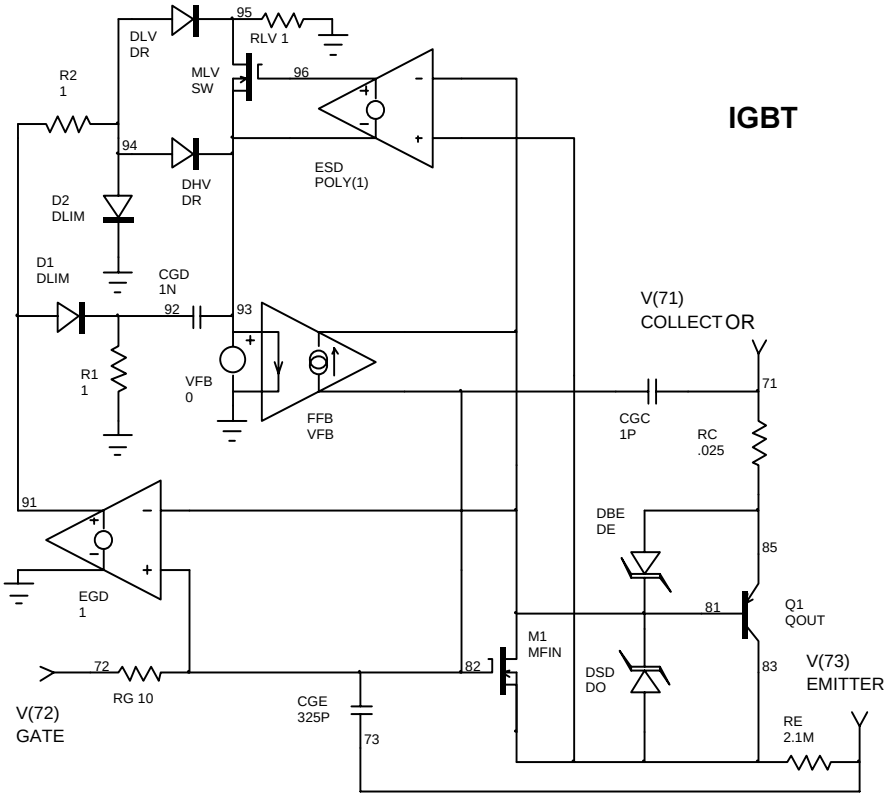
Darlington Transistor

Power MOSFET



SCR





Finding Out More About SPICE Model Parameters

Each SPICE model parameter has a specific meaning and a specific function. For a description of each SPICE parameter, please see the IsSpice4 manual and on-line help. The best general book on SPICE model parameter descriptions is titled “Semiconductor Device Modeling With SPICE”. However, it contains very little information on how to extract SPICE parameters from the data available in data sheets.

General Information, SPICE Parameters, SPICE Models

[1] Semiconductor Device Modeling With SPICE, P. Antognetti, G. Massobrio, McGraw-Hill, 1988

[2] Simulating With Spice, L.G. Meares, C.E. Hymowitz, Intusoft, 1988

[3] IsSpice4 User's Guide, Intusoft, 1990

[4] Handbook of Modeling for Circuit Analysis Including Radiation Effects, R. Simon, BDM Corp. Albuquerque, N.M., May 1979, Air Force Weapons Laboratory, AFWL-TR-79-86

Diodes and Bipolar Transistor Models

[1] Modeling The Bipolar Transistor, Ian Getrau, Tektronix Laboratories, Tektronix Inc., Beaverton, Oregon, Elsevier Scientific Publishing Company 1978

[2] An Integral Charge Control Model of the Bipolar Transistor, H.K. Gummel and H.C. Poon, Bell System Technical Journal, May-June 1970, pp827-54

[3] PreSpice User's Guide, Intusoft, 1990

JFETS and MOSFETS

[1] The Simulation of MOS Integrated Circuits Using Spice2, A. Vladimirescu, S. Liu, ERL Memo No. M80/7, U.C. Berkeley 1980

[2] FET Modeling For Circuit Simulation, Dileep A. Divekar, Kluwer Academic Press, 1988

[3] SPICE Models For Power Mosfets: An Update, H.P. Yee, Peter Lauritzen, 3rd Annual IEEE Applied Power Electron Conf. and Expo, New Orleans, 1988

[4] SPICE-2 Computer Models For HEXFETS, R.W. Negus, International Rectifier, Application Note 954, 1984

Chapter 12 - Testing SPICE Models

Testing SPICE Models

After testing a model or subcircuit you may find that your requirements have not been met by the data entered. For example, a plot of the DC characteristic of a BJT model may reveal that the output conductance in the saturated region does not correspond to the data sheet curves. Discrepancies such as this can be due to a number of factors. In any case, there are two ways to improve the desired characteristics of the model.

The first way to improve the performance of a model is to adjust the SpiceMod data entries to improve the response. This is the recommended method since changes in one data field may affect changes in another field. SpiceMod will account for any changes if the default values are used. Adjusting SpiceMod input values may be quite easy if the data sheet parameter has a clear effect on the generated test curve. For example, changing the Peak Current Gain (hFE) will directly affect the transistor's gain. In some cases, however, this direct link may not be available or evident.

If you leave SpiceMod to simulate a circuit and restart Spice-Mod to tweak a data sheet value, you must re-enter any data sheet values previous entered. Therefore, if you plan on tweaking your SPICE models, it is a good idea to record or print out the data sheet values that you entered when the original model was created.

The second method is to adjust the SPICE model parameters directly. This may be quite difficult if you do not understand the relationship between the SPICE parameters and the test circuit waveforms. In some cases, several parameters may be available to adjust the simulated response. Knowing which parameters affect the test curves, and how, will take some research and you should consult the references in the "Finding Out More About SPICE Model Parameters" section. The SpiceMod data entry screens will give an indication of which SPICE model parameter is most affected by each data sheet parameter .

Before tweaking any SPICE parameters or adjusting your SpiceMod data entries, you should ask yourself the following question. Is the model as accurate as it has to be for my application? If the answer is yes, then you should not spend any time improving the model.

Using The Test Circuits

Each test circuit contains several parts. The schematic will be shown along side a SPICE compatible netlist, displayed only for clarity. The netlist you actually simulate will be different. SPICE users should note that the netlists in the .CIR files may contain some unfamiliar statements. (*INCLUDE, *DEFINE, and *ALIAS). They are generated by SpiceNet. The statements begin with a comment delimiter and will not affect the SPICE simulation. Two separate sections will detail how to use the test circuits with the ViewAnalog simulation system and with SPICE standalone.

In each SPICE netlist, the .MODEL or .SUBCKT netlist and the corresponding model/subcircuit name being tested may appear in italics. When using the test circuits, you must insert the proper model or subcircuit statement into the netlist and make sure the calling statement (D, Q, J, M, or X) contains the correct model name. (replace the phrase DUT with the model name).

For SpiceNet users: You will have to replace the DUT device with the device you want to test.

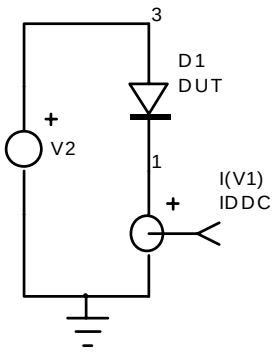
Important Note: Most of the test circuits require some information from the data sheet such as the device operating point. Others will require that the SPICE control statements be modified in order to produce results over the same interval contained in the data sheet. In either case, make sure that any specific test conditions used to generate the data sheet data are duplicated by the test circuits. Test circuits provided in data sheets can also be used to test your models.

Testing Diodes

There are three diode test circuits. They test the IV response, the reverse recovery time, and the junction capacitance versus reverse voltage. The circuits for the IV response and recovery time are shown separately, but are contained in one circuit file (Diodetst.Cir) so as to allow them to be simulated simultaneously.

Diode IV Curve

Current vs. Voltage Response




```
DIODETST - IV Curve Circuit with DN4148 Model
.DC VD 0 1.5 .01
.MODEL DN4148 D (IS=38.1N
+ RS=.521 N=2.09 BV=99.9 IBV=100N
+ CJO=4P VJ=.75 M=.333 TT=7.2N)
*ALIAS  I(V1)=IDDC
.PRINT DC  I(V1)
V1 1 0
VD 2 0
D1 2 1 DN4148
.END
```

In order to place the newly made SpiceMod model, you must update the SpiceNet database. See the SpiceNet on-line help for more information.

SpiceNet Users:

- Display the DIODETST schematic in SpiceNet.
- Replace the DUT device with the diode you want to simulate.
- In the Simulation Setup dialog, adjust the .DC statement to simulate the diode over the region of interest.
- Run the simulation.
- Run IntuScope and display the DC curve for IDDC (I(V1)) vs. VD equal to the diode current vs. diode voltage.

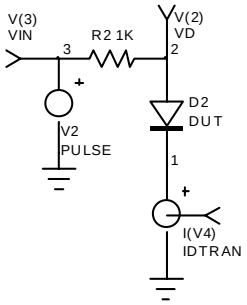
SPICE Only Users:

- Edit the DIODETST.CIR netlist with the editor you normally use to edit SPICE input netlists.
- At the end of the "D1" diode call statement, enter the name of the diode model that you want to simulate. For example, "D1 2 1 DN4148".
- Insert the .MODEL statement, corresponding to the model you just named, into the netlist.
- Adjust the .DC statement to simulate the diode over the region of interest.
- Run the simulation and observe the output file. The data will be listed under the DC Transfer Curves banner as I(V1) vs. VD.

SPICE MODEL Notes: Increasing IS or decreasing N will increase the diode current vs. voltage response. Increasing RS will increase the amount that the curve deviates from an ideal diode curve in the high current region.

Diode Reverse Recovery Time

Reverse Recovery Time Response




```
DIODETST - Reverse Recovery Time Portion
.TRAN .5N 100N
.MODEL DN4148 D (IS=38.1N
+ RS=.521 N=2.09 BV=99.9 IBV=100N
+ CJO=4P VJ=.75 M=.333 TT=7.2N)
*ALIAS  V(4)=VD
*ALIAS  V(10)=VIN
*ALIAS  I(V4)=IDTRAN
.PRINT TRAN  V(4)  V(10)  I(V4)
V4 6 0
R2 10 4 1K
V2 10 0 PULSE 10 -10 .02U 1P 1P
D2 4 6 DN4148
.END
```

SpiceNet Users:

- Display the DIODETST schematic in SpiceNet.
- Replace the DUT device with the diode you want to simulate.
- In the Simulation Setup dialog, adjust the .TRAN statement to simulate the diode over the region of interest.
- Adjust the PULSE statement in the V2 voltage source, if necessary. The data sheet may give some information on the voltage levels and time span to use.
- Run the simulation.
- Run IntuScope and display the curve IDTRAN, (diode current I(V4) vs. Time). VIN is the input voltage. VD is the diode voltage.

SPICE Only Users:

- Edit the DIODETST.CIR netlist with the editor you normally use to edit SPICE input netlists.
- At the end of the diode call statements, enter the name of the diode model that you want to simulate. For example, "D2 4 6 DN4148".

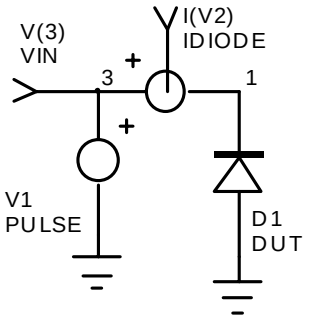
- Insert the .MODEL statement, corresponding to the model you just named, into the netlist.
- Adjust the .TRAN statement to simulate the diode over the region of interest.
- Adjust the PULSE statement in the V2 voltage source, if necessary. The data sheet may give some information on the voltage levels and time span to use.
- Run the simulation and observe the output file. The data will be listed under the Transient analysis banner as I(V4) vs. Time.

SPICE MODEL Notes: Increasing TT will increase the time it takes for the diode to turn off.

Diode Capacitance Characteristics

A simple test circuit can be used to create the CV characteristic. The circuit works by producing a voltage ramp from the source V1. Using the equation I=C dv/dt and solving for C we get C = I/dv/dt. Dividing the current through the diode by dv/dt, which is the slope of the ramp and a constant (=50/5U=10Meg), will produce the capacitance curve. Please see the section on "Adding More SPICE Parameters" for information on adjusting the SPICE model parameters to affect the CV response.

Capacitance vs. Reverse Voltage




```
D-CAP -  Diode Capacitance
.TRAN .01U 5U
.MODEL DN4148 D (IS=38.1N
+ RS=.521 N=2.09 BV=99.9 IBV=100N
+ CJO=4P VJ=.75 M=.333 TT=7.2N)
*ALIAS  I(V2)=IDIODE
*ALIAS  V(1)=VIN
.PRINT TRAN  I(V2) V(1)
V2 1 2
D1 0 2 DN4148
V1 1 0 PULSE 0 50 0 5U
.END
```

SpiceNet Users:

- Display the D-CAP schematic in SpiceNet. Replace the DUT device with the diode you want to simulate.
- Run the simulation.
- Enter IntuScope and select the Select X-Y... function under the WAVEFORMS menu.
- Display IDIODE (Y axis) vs. VIN (X axis). Type “1w10MEG/” to divide IDIODE by dv/dt (10Meg), and display the capacitance vs reverse voltage waveform.

SPICE Only Users:

- Edit the D-CAP.CIR netlist with the editor you normally use to edit SPICE input netlists.
- At the end of the “D1” diode call statement, enter the name of the diode model that you want to simulate. For example, “D1 0 2 DN4148”.
- Insert the .MODEL statement, corresponding to the model you just named, into the netlist.
- Run the simulation. The current, I(V2), divided by 10Meg, vs. the voltage, V1, is equal to the capacitance vs. reverse voltage.

Testing Bipolar Junction Transistors

There are five BJT test circuits. They consist of:

Filename	Description
BJTTST	Collector Characteristics, VCE vs. IC
VBEIC	Transconductance, VBE vs. IC
QSAT	VBE and VCE Saturation Curves
BJT-CAP	CB and BE Junction Capacitances
TONTOFF	Switching Test circuit - Tr, Td, Tf, Ts

The test circuits are setup to be used with the standard BJT NPN .MODEL statement created by the “Bipolar Junction Transistor” screen in SpiceMod. The schematic and .CIR files contain notes on how to alter the circuits for use with PNP devices. The test circuits can also be used with either the Power Transistor or Darlington Transistor subcircuits.

For those who are using SPICE stand alone:

These two sections also apply to the Mosfet/power Mosfets test circuits.

To use the test circuits with Power or Darlington BJTs

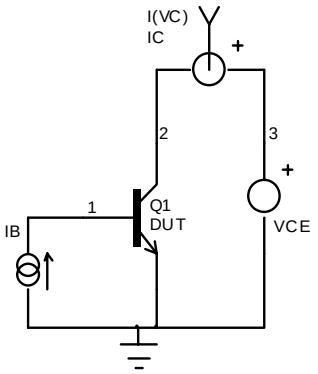
- Go into the .CIR netlist and replace or comment out any bipolar transistor call statements that begin with the letter Q. Then, re-enter the same statements on a new line, except begin the line with the letter X instead of the letter Q. Continue as described in each section.

  For example.: Replace ***Q1*** 1 2 3 ***MPS3903***
  With ***X1*** 1 2 3 ***TIP141***

- Do not change the node numbers. Make sure to enter the subcircuit name at the end of the line in place of the model name that was used with the Q statement.

BJT Collector Characteristics

VCE vs. IC for several values of IB




```
BJTTST - Collector Characteristics
.DC VCE 0  15  .5  IB  100U  500U  100U
*Set the range for VCE and IB above
*For PNP devices flip IB, VC, and VCE
.MODEL MPS3903 NPN (IS=.937F NF=1
+ BF=445 VAF=113 IKF=70M ISE=2.71P
+ NE=2 BR=4 NR=1 VAR=16 RE=1.81
+ RB=7.26 RC=.726 XTB=1.5 CJE=8.17P
+ CJC=5.10P TF=636P TR=297N)
*ALIAS  I(VC)=IC
.PRINT DC  I(VC)
IB 0 1
Q1 2 1 0 MPS3903
*Use "X1 2 1 0 SubName" above to
*test Power or Darlington Transistors
VC 3 2
VCE 3 0
.END
```

SpiceNet Users:

- Display the BJTTST schematic in SpiceNet.
- Replace the DUT device with the BJT you want to simulate.
- In the Simulation Setup dialog, adjust the .DC statement to simulate the BJT over the desired region.
- Run the simulation.
- Run IntuScope and display the DC curve IC vs. VCE for various values of IB.

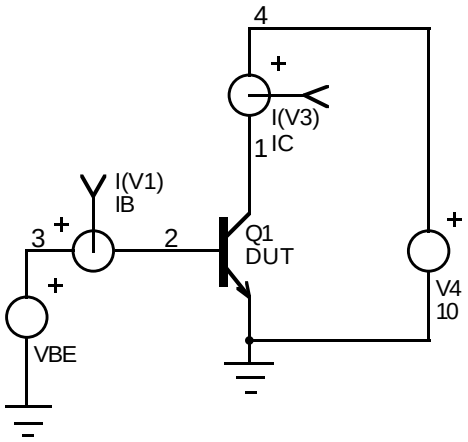
SPICE Only Users:

- Edit the BJTTST.CIR netlist with the editor you normally use to edit SPICE input netlists.
- At the end of the “Q1” call statement, enter the name of the BJT model that you want to simulate. For ex., “Q1 2 1 0 MPS3903”.

- Insert the .MODEL statement, corresponding to the model you just named, into the netlist.
- Adjust the >DC statement to simulate the BJT over the region of interest.
- Run the simulation and observe the output file. The data will be listed under the DC analysis banner as I(VC) vs. VCE.

Notes: For PNP devices, flip (interchange node numbers) the sources VBE, V1, V4, and V3 (labeled as I(V3). For power and Darlington transistors, replace the "Q1 2 1 0 model_name" line with "X1 2 1 0 Subcircuit_name" and append the proper subcircuit netlist.

BJT Transconductance




```
VBEIC - IC and IB vs. VBE Circuit
.MODEL MPS3903 NPN (IS=.937F NF=1
+ BF=445 VAF=113 IKF=70M ISE=2.71P
+ NE=2 BR=4 NR=1 VAR=16 RE=1.81
+ RB=7.26 RC=.726 XTB=1.5 CJE=8.17P
+ CJC=5.10P TF=636P TR=297N)
DC VBE .1 .14 .05
Adjust .DC statement ot achieve correct range
For PNP devices flip VBE, V1, VCE and V3
*ALIAS  I(V1)=IB
*ALIAS  I(V3)=IC
.PRINT DC  I(V1) I(V3)
V1 2 3
VBE 2 0
V3 4 1
VCE 4 0 10
*Adjust VCE voltage if necessary
Q1 1 3 0 MPS3903
.END
```

SPICE Only Users:

- Display the VBEIC schematic in SpiceNet.
- Replace the DUT device with the BJT you want to simulate.

- In the Simulation Setup dialog, adjust the .DC statement to simulate the BJT over the proper region.
- Run the simulation.
- Run IntuScope and display the DC curve for IC vs. VBE.

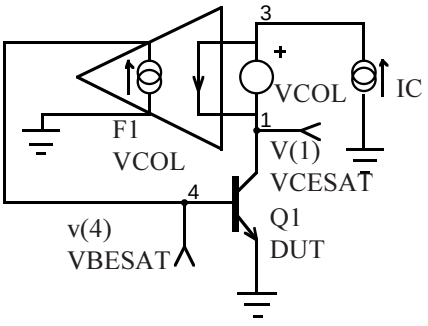
SPICE Only Users:

- Edit the VBEIC.CIR netlist with the editor you normally use to edit SPICE input netlists.
- At the end of the “Q1” BJT statement, enter the name of the BJT model that you want to simulate. For ex., “Q1 1 3 0 MPS3903”.
- Insert the .MODEL statement, corresponding to the model you just named, into the netlist.
- Adjust the .DC statement to simulate the BJT over the region of interest.
- Run the simulation and observe the output file. The data will be listed under the DC transfer curves banner as IC vs. VBE.

Notes: For PNP devices, flip (interchange node numbers) the sources VBE, V1, V4, and V3 (labeled as I(V3). For power and Darlington transistors, replace the “Q1 1 3 0 model_name” line with “X1 1 3 0 Subcircuit_name” and append the proper subcircuit netlist.

BJT Saturation Characteristics

VCE(SAT) and VBE(sat) vs. IC




```
QSAT-BJT Saturation Voltages
*VCE(SAT)=v(4) VS. IC, VBE(SAT)=V(2) VS. IC
.OPTIONS RELTOL=.0001
.MODEL MPS3903 NPN (IS=.937F NF=1
+ BF=445 VAF=113 IKF=70M ISE=2.71P
+NE=2 BR=4 NR=1 VAR=16 RE=1.81
+RB=7.26 RC=.726 XTB=1.5 CJE=8.17P
+CJC=5.10P TF=636P TR=297N)
.DC IC 1M 100M 1M
*Replace ICLO and ICHI with data sheet range
*ALIAS V(4)=VCESAT
*ALIAS V(2)=VBESAT
.PRINT DC V(4) V(2)
IC 0 1
F1 0 2 VCOL .1
*I(VCOL)=IC In, IB=IC/10 OUT
VCOL 1 4
Q1 4 2 0 MPS3903
.END
```

SpiceNet Users:

- Display the QSAT schematic in SpiceNet.
- Replace the DUT device with the BJT you want to simulate.
- In the Simulation Setup dialog, adjust the .DC statement to Simulate the BJT over the proper region.
- Run the simulation.
- Run IntuScope and display the DC curve for VCESAT vs. IC and VBESAT vs. IC

SPICE Only Users:

- Edit the QSAT.CIR netlist with the editor you normally use to edit SPICE input netlists.
- At the end of the “Q1” call statement, enter the name of the BJT model that you want to simulate. For ex., “Q1 4 2 0 MPS3903”.

- Insert the .MODEL statement, corresponding to the model you just named, into the netlist.

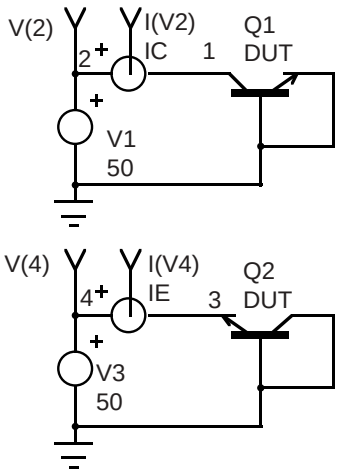
- Adjust the .DC statement to simulate the diode over the region of interest.

- Run the simulation and observe the output file. The data will be listed under the DC transfer curves banner as V(4) (VCEsat) vs. IC and V(2) (VBEsat) vs. IC

Notes: For PNP devices, flip (interchange node numbers) the source IC. VCE(sat) vs. IC will equal -V(4) vs. IC, VBE(sat) vs. IC will equal -V(2) vs. IC. For power and Darlington transistors, replace the “Q1 4 2 0 model_name” line with “X1 4 2 0 Subcircuit_name” and append the proper subckt netlist.

BJT Capacitance Characteristics

Collector-Base and Base-Emitter Capacitance




```
BJT-CAP - Capacitance vs. Reverse Voltage
.TRAN .02U 5U
.MODEL MPS3903 NPN (IS=.937F NF=1
+BF=445 VAF=113 IKF=70M ISE=2.71P
+NE=2 BR=4 NR=1 VAR=16 RE=1.81
+RB=7.26 RC=.726 XTB=1.5 CJE=8.17P
+CJC=5.10P TF=636P TR=297N)
*ALIAS I(V2)=IC
*ALIAS I(V4)=IE
.PRINT TRAN I(V2) V(2) I(V4) V(4)
V1 2 0 50 PUSE 0 50 0 5U
V2 2 1
Q2 0 0 3 MPS3903
V3 4 0 50 PULSE 0 50 0 5U
V4 4 3
Q1 1 0 0 MPS3903
.END
```

SpiceNet Users:

- Display the BJT-CAP schematic in SpiceNet.

- Replace the DUT device with the BJT you want to simulate.

- Run the simulation.
- Enter IntuScope and select the Select X-Y... function under the WAVEFORMS menu.
- Display IC (Y axis) vs. VIN (X axis). Type “1w10MEG/” to divide IC by dv/dt (10Meg), and display the Cob vs reverse voltage waveform. Do the same for IE vs. VIN to display Cib.

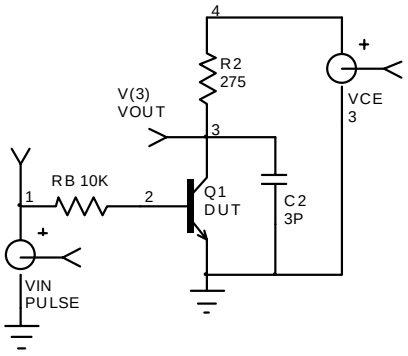
SPICE Only Users:

- Edit the BJT-CAP.CIR netlist with the editor you normally use to edit SPICE input netlists.
- At the end of both BJT (Q) call statements, enter the name of the BJT model that you want to simulate.
- Insert the .MODEL statement, corresponding to the model you just named, into the netlist.
- Run the simulation. The current, I(V2) [I(V4)], divided by 10Meg, vs. the voltage, V1, is equal to Cob [Cib] vs. Vreverse.

Notes: See the diode capacitance circuit for an explanation of the operation of this circuit. Please see the section on “Adding More SPICE Parameters” for information on adjusting the capacitance response. This circuit may be adapted for PNP devices by flipping (interchange node numbers) the sources V1, V2, V3, and V4. For power and Darlington Transistors, replace the “Q2 0 0 3 model_name” and “Q1 1 0 0 model_name” lines with “X2 0 0 3 Subcircuit_name” and “X1 1 0 0 Subcircuit_name”, respectively and append the proper subcircuit netlist.

BJT Switching Characteristics

Switching Test Circuit




```
TONTOFF - Switching Waveform
.TRAN 2N 600N
*Adjust data printout interval and total time
*Add .MODEL statement
*ALIAS  V(3)=VOUT
*ALIAS  V(1)=VIN
.PRINT TRAN  V(3)  V(1)  I(VIN) I(VCE)
RB 1 2 10K
*RB 1 2 _RB, Replace _RB with data sheet value
Q1 3 2 0 MPS3903
R2 3 4 275
*R2 3 4 _RL, Replace _RL w/load resistance
VCE 4 0 3
*VCE 4 0 _V, Replace _V with data sheet value
C2 3 0 3P
VIN 1 0 PULSE -9.1 10.9 0 .1N .1N 300NS 600NS
*               Init Final Delay Rise Fall Width Period
.END
```

SpiceNet Users:

- Display the TONTOFF schematic in SpiceNet.
- Replace the DUT device with the BJT you want to simulate.
- In the Simulation Setup dialog, adjust the .TRAN statement to simulate the BJT over the proper region.
- In the netlist adjust RB, R2, VIN, VCE and the Pulse statement. Use data sheet info if available.
- Run the simulation. Run IntuScope and display the Transient curve for VOUT. Tr, Td, Tf, and Ts can then be measured.

SPICE Only Users:

- Edit the TONTOFF.CIR netlist with the editor you normally use to edit SPICE input netlists.
- At the end of the “Q1” call statement, enter the name of the BJT model that you want to simulate. For ex., “Q1 3 2 0 MPS3903”.

- Insert the .MODEL statement, corresponding to the model you just named, into the netlist.
- Adjust the .TRAN statement to simulate the BJT over the proper region. Adjust RB, R2, VIN, VCE and the Pulse statement. Use data sheet info.
- Run the simulation and observe the output file. The data will be listed under the Transient analysis banner as V(3) vs. Time.

Notes: For PNP devices, flip (interchange node numbers) the source VIN. For power and Darlington transistors, replace the "Q1 3 2 0 model_name" line with "X1 3 2 0 Subcircuit_name" and append the proper subcircuit netlist.

Testing JFETS

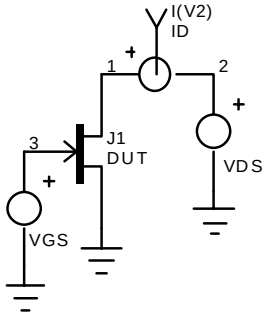
There are two JFET test circuits. They consist of:

Filename	Description
JFETTST	Output Characteristics, ID vs. VDS
JFETRDS	Drain Source on resistance, rDS

JFET Output Characteristics

SpiceNet Users:

ID vs. VDS for various values of VGS




```
JFETTST - Output Characteristics
.DC VDS 0 2 .2 VGS 0 -8 -1
*Set VDS and VGS range above
.MODEL J105 NJF (VTO=-7.25 BETA=5M
+LAMBDA=.035 RD=.42 RS=.378 IS=.948F
+PB=1 FC=.5 CGS=80P CGD=140P)
*ALIAS  I(V2)=ID
.PRINT DC  I(V2)
V2 2 1
VDS 2 0
J1 1 3 0 J105
VGS 3 0
.END
```

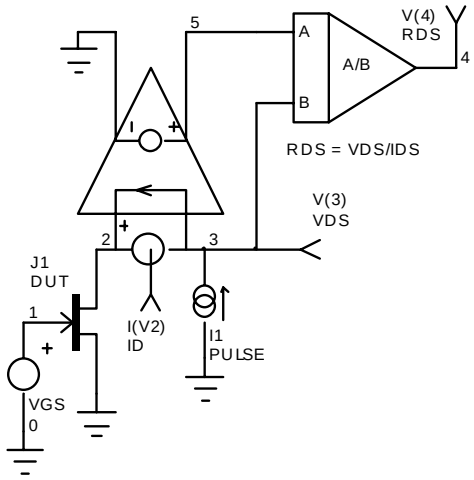
- Display the JFETTST schematic in SpiceNet.
- Replace the DUT device with the JFET you want to simulate.
- In the Simulation Setup dialog, adjust the .DC statement to simulate the JFET over the proper region.
- Run the simulation. Run IntuScope and display the DC curve for ID vs. VDS for various values of VGS.

SPICE Only Users:

- Edit the JFETTST.CIR netlist with the editor you normally use to edit SPICE input netlists.
- At the end of the "J1" statement, enter the name of the JFET model that you want to simulate. For ex., "J1 1 3 0 J105".
- Insert the .MODEL statement, corresponding to the model you just named, into the netlist.
- Adjust the .DC statement to simulate the JFET over the region of interest.
- Run the simulation and observe the output file. The data will be listed under the DC transfer curves banner as I(V2) vs. VDS.

JFET On Resistance Characteristics

rDS vs IDrain




```
JFETRDS - rdson Circuit
.TRAN .01 1
*ALIAS  I(V2)=ID
*ALIAS  V(4)=RDS
*ALIAS  V(3)=VDS
.PRINT TRAN  I(V2) V(4)  V(3)
V2 3 2
J1 2 1 0 Device_model_name
*Add device model
H1 5 0 V2 1
X1 3 5 4 DIVIDE
*************************
.SUBCKT DIVIDE 1 2 4
*Behavioral Model of a voltage divider.
* V(4) = V(1) / V(2), Vout=VA/VB
R1 1 0 1MEG
R2 2 0 1MEG
R4 4 0 1MEG
G1 0 3 1 0 1
G2 3 0 POLY(2) 2 0 3 0 0 0 0 0 1
R3 3 0 100MEG
E1 4 0 3 0 1
.ENDS
*************************
I1 0 3 PULSE 10M 300M 0 1
*Adjust Pulse values for correct response
VGS 1 0 0
*Adjust VGS to data sheet specification
.END
```

SpiceNet Users:

- Display the JFETRDS schematic in SpiceNet.
- Replace the DUT device with the JFET you want to simulate.
- Adjust the initial and final values in the I1 PULSE statement to the initial and final ID data sheet values. Adjust VGS.
- Run the simulation.
- Run IntuScope and display an X-Y plot of RDS vs. ID.

SPICE Only Users:

- Edit the JFETRDS.CIR netlist with the editor you normally use to edit SPICE input netlists.
- At the end of the "J1" statement, enter the name of the JFET model that you want to simulate. For ex., "J1 2 1 0 J105".
- Insert the .MODEL statement, corresponding to the model you just named, into the netlist.
- Adjust the initial and final values in the I1 PULSE statement to the initial and final ID data sheet values. Adjust VGS.
- Run the simulation and observe the output file. The data will be listed under the Transient analysis banner as V(4) vs. I(V2).

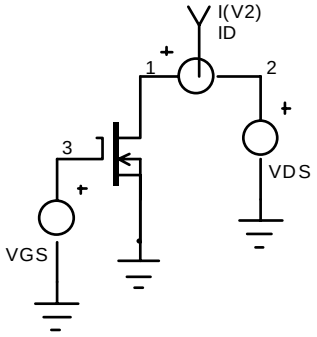
Testing MOSFETs

There are three MOSFET test circuits. They consist of:

Filename	Description
MOSCURVS	Output Characteristics, ID vs. VDS
MOSCAP	Capacitance, Coss, Ciss, Crss
MOSSWTCH	Inductive/Resistive Switching

MOSFET Output Characteristics

ID vs. VDS for various values of VGS




```
MOSCURVS - MOSFET Input/Output Curves
*DEFINE DUT=IRF450
*INCLUDE POWMOS.LIB
*For P-channel FETS flip VGS, VDS, AND V2.
.DC VDS .5 20 .1 VGS 5 10 1
*Set drain and gate voltage ranges.
*.DC VGS 5 20 .2
*For ID VS. VGS, use .DC VGS , plot I(V2) vs. VGS.
*ALIAS  I(V2)=ID
.PRINT DC I(V2) V(3)
V2 2 1
VDS 2 0 100
VGS 3 0 0
X1 1 3 0 DUT
*For small signal MOSFETS replace X1 with M1
.END
```

SpiceNet Users:

- Display the MOSCURVS schematic in SpiceNet.
- Replace the DUT device with the MOSFET you want to simulate.
- Adjust the .DC statement VDS and VGS values to simulate the FET over the proper region.
- Run the simulation.
- Run IntuScope and display the DC curve for ID vs. VDS.

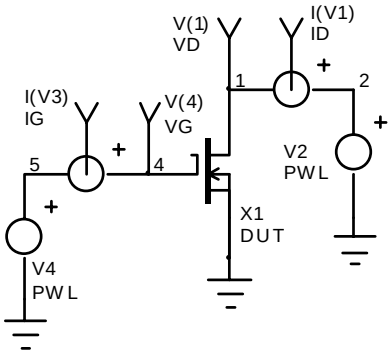
SPICE Only Users:

- Edit MOSCURVS.CIR with your SPICE input netlist editor.
- At the end of the "X1" statement, enter the name of the power Mosfet model that you want to simulate. For example, "X1 1 3 0 IRF150". Insert the .SUBCKT netlist, corresponding to the device you just named, into the netlist.
- Adjust the .DC statement VDS and VGS values to simulate the FET over the proper region.
- Run the simulation and observe the output file. The data will be listed under the DC analysis banner as I(V2) vs. VDS.

Notes: For PMOS devices, flip (interchange node numbers) VDS, VGS, and V2. For Mosfet (MOSFET (M)) models that use a .MODEL statement, replace the "X1 1 3 0 Sub_name" line with "M1 1 3 0 0 Model_name" and append the proper .model netlist. Note, the added 0 node number for the Mosfet substrate connection. SpiceNet users may simply replace the X1 Power Mosfet symbol with any standard small signal Mosfet symbol.

MOSFET Capacitance Characteristics

Crss, Coss, Ciss vs. Forward/Reverse Voltage




```
MOSCAP.CIR - MOS-FET Capacitance Curves
*DEFINE DUT=IRF150
*REPLACE DUT= WITH DUT=MODELNAME
*INCLUDE POWMOS.LIB
.PRINT TRAN V(1,4) I(V3) I(V1)
*USE V(4,1) FOR PMOS DEVICES
*ALIAS V(1,4)=VDG
.TRAN .5U 70U
*FOR PMOS DEVICES FLIP V1, V2, V3, V4
*ALIAS  I(V3)=IG
*ALIAS  I(V1)=ID
*ALIAS  V(4)=VG
*ALIAS  V(1)=VD
.PRINT TRAN  I(V3) I(V1) V(4)  V(1)
V1 2 1
V2 2 0 PWL 0U 0V, 20U 0V, 70U 50V
V3 4 5
V4 5 0 PWL 0U 20V, 20U 0V
X1 1 4 0 DUT
.END
```

For better MOSFET capacitance curves set VTO=20 and remove the source lead inductance.

SpiceNet Users:

- Display the MOSCAP schematic in SpiceNet.
- Replace the DUT device with the MOSFET you want to simulate.
- Run the simulation.
- Run IntuScope. Display an X-Y plot of ID vs. VDG. Type in “1w10MEG/” to divide ID by dv/dt (10Meg), and display Ciss. Do the same for IG vs. VDG = Crss. Coss will equal Ciss-Crss.

The MOSCAP test circuit can also be used to test IGBTs. V(1,4)=VCG I(V1)=IC V(1)=VC.

SPICE Only Users:

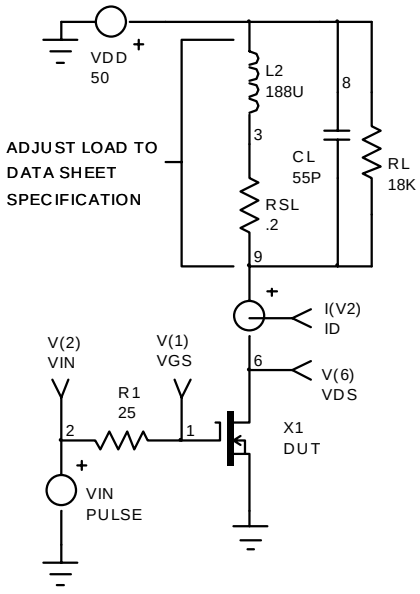
- Edit the MOSCAP.CIR netlist with your SPICE input netlist editor.
- At the end of the “X1” statement, enter the name of the MOSFET model that you want to simulate.
- Insert the .SUBCKT statement, corresponding to the device you just named, into the netlist.

- Run the simulation and observe the output file. The data will be listed under the transient analysis. Ciss equals I(V1)/10Meg vs. V(1,4). Crss equals I(V3)/10Meg vs. V(1,4). Coss equals Ciss - Crss.

Notes: The curves will display the capacitance in the forward bias region (-20V < VGS < 0) and reverse bias region (0 < VDS < 50). For PMOS devices, flip (interchange node numbers) V1, V2, V3, and V4. Use .PRINT TRAN V(4,1) for the voltage specification (X axis). For Mosfet (MOSFET (M)) models that use a .MODEL statement replace the "X1 1 4 0 Sub_name" line with "M1 1 4 0 0 Model_name" and append the proper .model netlist. Note, the added 0 node number for the Mosfet substrate connection.

MOSFET Switching Characteristics

Switching Test Circuit




```
Mosswtch Circuit - Mosfet Switching Characteristics
*Make sure to adjust the load values and configuration.
*INCLUDE MOSFET.LIB
*MAKE SURE TO USE THE CORRECT LIBRARY
*DEFINE DUT=IRF150
*REPLACE DUT= WITH DUT=MODELNAME
.TRAN 50N 10U
*ADJUST THE DATA  INTERVAL AND TOTAL TIME
*FOR PMOS DEVICES FLIP VIN AND ADJUST VDD
*ALIAS  I(V2)=ID
*ALIAS  V(1)=VGS
*ALIAS  V(6)=VDS
*ALIAS  V(2)=VIN
.PRINT TRAN  I(V2) V(1)  V(6)  V(2)
R1 1 2 25
*ADJUST TO DATA SHEET SPECIFICATION
RSL 3 9 .2
CL 8 9 55P
RL 8 9 18K
V2 9 6
VDD 8 0 50
*SET VDD PER DATA SHEET
VIN 2 0 PULSE 0 10 500N 1N 1N 2U 10U
*ADJUST INPUT PULSE PER DATA SHEET
L2 8 3 188U
X1 6 1 0 DUT
.END
```

Comparison of VDS [V(6)] and VIN [V(2)] will allow Tr, Tf, Td and TS to be calculated.

SpiceNet Users:

- Display the MOSSWTCH schematic in SpiceNet. Replace the DUT device with the MOSFET you want to simulate.
- Adjust the values for VIN, R1, VDD and the load to the data sheet specification.
- Run the simulation. Run IntuScope and display the Transient curve for VIN and VDS vs. Time.

SPICE Only Users:

- Edit the MOSSWTCH.CIR netlist with the editor you normally edit SPICE input netlists with.
- At the end of the "X1" statement, enter the name of the MOSFET subcircuit that you want to simulate. Insert the .SUBCKT netlist, corresponding to the device you just named, into the netlist.
- Adjust the .TRAN statement to simulate the MOSFET over the proper region. Adjust the values for VIN, R1, VDD and the load to the data sheet specification.
- Run the simulation and observe the output file. The data will be listed under the Transient analysis banner as V(6) [VDS] vs. Time.

Switching Test Circuit Notes

Parasitic variations can have dramatic effects on the simulation results.

The preceding circuit can be used to check the switching characteristics using either resistive or inductive loading, with or without diode clamping. Some simple additions or alterations, however, may be required. Most data sheets will give some indication of the circuit requirements including the component values for the load and base test circuit, the voltage levels, and the timing requirements.

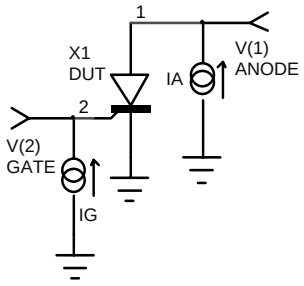
If inductive loading is used, as shown in the schematic, the user should be careful to model the load as accurately as possible before comparing the simulated data with the data sheet data.

Testing SCRs

There are two SCR test circuits. They consist of:

Filename	Description
SCRDC	Breakdown, On-voltage
SCRDVDT	dv/dt turn-on test

SCR DC Characteristics




```
SCRDC - SCR DC CURVES
* For testing SCR dc characteristics
*INCLUDE SCR.LIB
*       ^Use the correct .LIB file name
*DEFINE DUT=SN4171
*          ^Use the correct model name
.DC IA -.1 .1 .001 IG 0 .02 .02
*       ^Change as per the breakdown voltage curve
*.DC IA 0 100 1
*       ^Change as per the ON-voltage data sheet curve
*ALIAS  V(1)=ANODE VOLTAGE
*ALIAS  V(2)=GATE VOLTAGE
.PRINT DC  V(1)  V(2)
IA 0 1 1
IG 0 2 .02
*      ^CHANGE TO BIAS THE SCR
X1 1 2 0 DUT
.END
```

The range of the .DC statement will determine the simulation results.

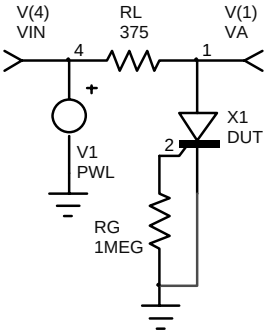
SpiceNet Users:

- Display the SCRDC schematic in SpiceNet. Replace the DUT device with the SCR you want to simulate.
- In the Simulation Setup dialog, set the .DC statement to control the gate current and anode current. Depending on the range of IA selected, the breakdown or forward saturation voltage will be produced.
- Run the simulation. Run IntuScope. Display the V(1) waveform equal to the anode voltage.

SPICE Only Users:

- Edit the SCRDC.CIR netlist with your SPICE input netlist editor.
- At the end of the "X1" statement, enter the name of the SCR model that you want to simulate.
- Insert the .SUBCKT statement, corresponding to the device you just named, into the netlist.
- Set the .DC statement to control the gate current and anode current. Depending on the range of IA selected, the breakdown or forward saturation voltage will be produced.
- Run the simulation and observe the output file. The data will be listed under the DC Sweeps analysis banner as V(1) [VA] vs. IA.

SCR dv/dt Turn-on




```
SCRDVDT - SCR dv/dt test circuit
*INCLUDE SCR.LIB
*       ^Use the correct .LIB file name
*DEFINE VOLT=500
*           ^Set to above breakover voltage
*DEFINE TIME=5U
*           ^Set for dv/dt with volt/time
.TRAN .05U TIME
*DEFINE DUT=SN4171
*           ^Replace with correct model name
*ALIAS  V(1)=VA
*ALIAS  V(4)=VIN
*ALIAS  I(V2)=IA
.PRINT TRAN  V(1)  V(4)  I(V2) @RL[i]
RL 4 1 375
*     ^USE RL=10 * VMAX/IMAX
X1 1 2 0 DUT
RG 2 0 1MEG
*     ^USE SPECIFIED GATE LOAD (1MEG=OPEN)
V1 4 0 PWL 0 0 TIME VOLT
.END
```

SpiceNet Users:

- Display the SCRDVDT schematic in SpiceNet.

This circuit supplies a dv/dt ramp extending above the breakover voltage to the anode. The SCR should not turn on until the breakover voltage is reached. A dv/dt above rating should cause earlier turn-on.

- Replace the DUT device with the SCR you want to simulate.
- In the Simulation Setup dialog, adjust the value of VOLT and TIME to produce the correct driving voltage waveform. Adjust RL and RG if necessary.
- Run the simulation.
- Run IntuScope. Display VA=V(1), the anode voltage.

SPICE Only Users:

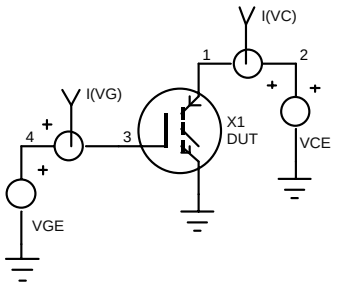
- Edit the SCRDVDT.CIR netlist with your SPICE input netlist editor.
- At the end of the "X1" statement, enter the name of the SCR model that you want to simulate.
- Insert the .SUBCKT statement, corresponding to the device you just named, into the netlist.
- Enter the Simulation Setup dialog and enter the name of the model you want to simulate in the ∗DEFINE statement. Adjust the Library name in the ∗INCLUDE statement if necessary.
- Also in the Simulation Setup dialog, adjust the value of VOLT and TIME to produce the correct driving voltage waveform. Adjust RL and RG if necessary.
- Run the simulation.
- Run IntuScope. Display VA=V(1), the anode voltage.

Testing IGBTs

There are two IGBT test circuits. They consist of:

Filename	Description
IGBTDC	Output Characteristics, IC vs. VCE
IGBTTRAN	Switching Times

IGBT DC Characteristics




```
IGBTDC - IGBT Output Characteristics
*INCLUDE IGBT.LIB
*       ^Use the correct .LIB file name
*DEFINE DUT=IRGBC40U
*          ^Use the correct subcircuit name
.DC VCE 1 20 .1 VGE 5 10 1
*       ^Adjust the drain and gate voltage ranges
*.DC VGE 5 20 .2
.OPTIONS ITL1=300 ITL2=200
.PRINT DC  I(VG) I(VC)
VCE 2 0
VC 2 1
VG 4 3
VGE 4 0
X1 1 3 0 DUT
.END
```

For IC vs. VGE curve use .DC VGE only, Plot I(V2) vs. VGE

SpiceNet Users:

- Display the IGBTDC schematic in SpiceNet. Replace the DUT device with the IGBT you want to simulate.
- Adjust the .DC statement to simulate the IGBT over the region of interest. Run the simulation. Run IntuScope and display the DC curve I(VC) vs. VCE for various values of VGE.

SPICE Only Users:

Use the MOSFET capacitance test circuit to test the IGBT capacitance.

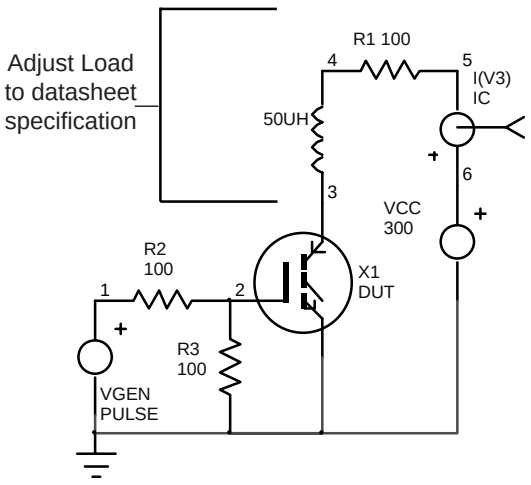
- Edit the IGBTDC.CIR netlist with your SPICE input netlist editor. At the end of the “X1” statement, enter the name of the IGBT model that you want to simulate. Insert the .SUBCKT statement, corresponding to the device you just named, into the netlist.
- Adjust the .DC statement to simulate the IGBT over the region of interest. Run the simulation and observe the output file. The data will be listed under the DC analysis banner as I(VC) vs. VCE.

IGBT Switching Characteristics

SpiceNet Users:

- Display the IGBTTRAN schematic in SpiceNet.

IGBT Switching Characteristics




```
IGBTTRAN - IGBT Switching Test Circuit
*INCLUDE IGBT.LIB
*DEFINE DUT=IRGBC40U
*          ^Use the correct subcircuit name
.TRAN 1N 1000N
*     ^Adjust the data step and total time
*ALIAS  V(5)=VGE
*ALIAS  I(V3)=IC
*ALIAS  V(1)=VCE
.PRINT TRAN  V(5)  I(V3) V(1)
L1 1 2 50UH
R1 2 3 100
VCC 6 0 300
VGEN 4 0 PULSE 0 20 1N 1N 500N 1U
R2 4 5 100
R3 5 0 100
V3 6 3
X1 1 5 0 DUT
.END
```

The IGBT load circuit configuration and values must be adjusted to obtain the correct data sheet response.

- Replace the DUT device with the IGBT you want to simulate.
- Adjust the .TRAN statement to simulate the IGBT over the region of interest. Adjust the VGEN PULSE source, the source resistance R2, and the IGBT load circuit.
- Run the simulation.
- Run IntuScope. The VGE, IC, and VCE responses will all be available.

SPICE Only Users:

- Edit the IGBTTRAN.CIR netlist with your SPICE input netlist editor.
- At the end of the “X1” statement, enter the subcircuit name of the IGBT that you want to simulate. Insert the .SUBCKT statement, corresponding to the device you just named, into the netlist.
- Adjust the .TRAN statement to simulate the IGBT over the region of interest. Adjust the VGEN PULSE statement, the source resistance R2, and the IGBT load circuit.
- Run the simulation and observe the output file. The data will be listed under the Transient analysis banner as V(5)=VGE, V(1)=VCE, and I(V3)=IC.

Chapter 13 - Adding More SPICE Parameters

Calculating Charge Storage Parameters

The charge storage parameters are extremely important for proper transient simulation of a device. For a diode, the main IsSpice4 parameters governing charge storage are CJO, the junction capacitance at zero bias, VJ, the built-in junction potential, and M the junction grading coefficient. BJT capacitance parameters are similar with a set for the collector-base (CJC, VJC, MJC) and base emitter (CJE, VJE, MJE) junctions.

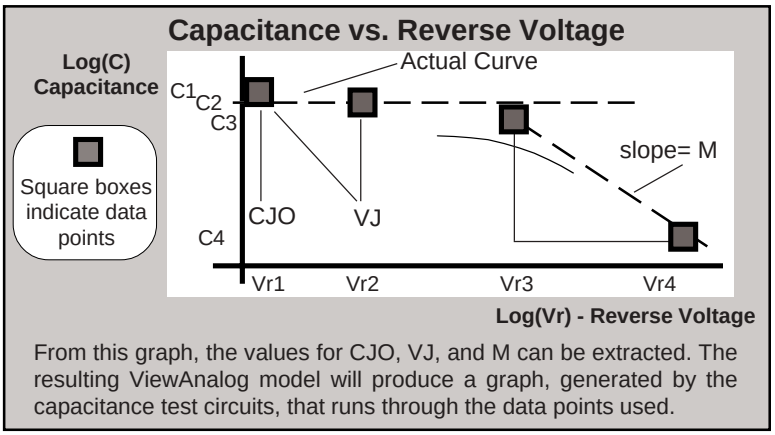
The pn junction capacitance response is described by:

For Reverse Bias: when VD - FC∗VJ	**For Forward Bias: when VD > FC∗VJ**
$CD = \frac{CJO}{\left[1 - \frac{VD}{VJ}\right]^{M}}$	$CD = \frac{CJO}{(1-FC)^{(1+M)}}\left(1 - FC(1+M) + M\frac{VD}{VJ}\right)$

The diode capacitance equations are shown above, but bipolar junction capacitances are similarly described by inserting the appropriate set of parameters. FC is normally left at the default value since forward bias data is almost never available.

SpiceMod will calculate the values for the zero bias junction capacitance parameter and the transit times. However, since a capacitance versus reverse voltage data curve is not usually available, the values for the junction potential and grading

coefficient are left at their default values. They will be accurate enough for most cases. VJ is typically between .2 and 1V, while M is .333 for a linear graded junction and .5 for a step graded junction. If the capacitance versus reverse voltage curve is available, the following procedure can be used to extract the



From this graph, the values for CJO, VJ, and M can be extracted. The resulting ViewAnalog model will produce a graph, generated by the capacitance test circuits, that runs through the data points used.

- M is the slope of the log(C) vs. log(Vr) curve at a point in the high reverse voltage region. The equation for M can be used assuming VJ is very small (0) compared to VD). The curve may have to be extrapolated to a higher voltage value than is shown on the graph.

$$M = \frac{\log(C4) - \log(C3)}{\log(Vr4 + VJ) - \log(Vr3 + VJ)}$$

- VJ is computed using two data points, one near Vr = 0:

$$VJ = \frac{\left[Vr\ 2 * \left(\frac{C\ 1}{C\ 2} \right)^{\frac{-1}{M}} - Vr\ 1 \right]}{\left[1 - \left(\frac{C\ 1}{C\ 2} \right)^{\frac{-1}{M}} \right]}$$

- Finally, CJO is computed at one data point near Vr = 0.

$$CJO = \frac{C1}{\left[\left(1 + \frac{Vr1}{VJ} \right)^{M} \right]}$$

For example, using CV data points **1** (7.5PF,.01V), **2** (6PF,.5V) **3** (3.5PF, 5V), and **4** (1.7PF, 50V) would produce:

M = log (3.5PF/1.7PF)/ log (50/5) = log(2.0588)/1 = **.3136**
VJ = [.5(7.5/6)$^{-3.188}$ - .01] / [1 - (7.5/6)$^{-3.188}$] = **.4625**
CJO = 7.5PF / (1+.01/.4625)$^{-.3136}$ = **7.55PF**

charge storage parameters for both diodes and all BJT's.

Calculating Noise Parameters

IsSpice4 accounts for noise generated by resistors and semiconductors. Resistors generate thermal noise, while semiconductors generate shot and flicker noise along with thermal noise if any model parameters for ohmic resistance are included. Shot noise is associated with the flow of direct current and is a function of the circuit configuration and the device's bias point. The amount of flicker noise exhibited by the device is controlled by two IsSpice4 model parameters, AF and KF. SpiceMod does not alter the AF and KF default values. They can, however, be calculated and added to any semiconductor .MODEL statement using the following procedure.

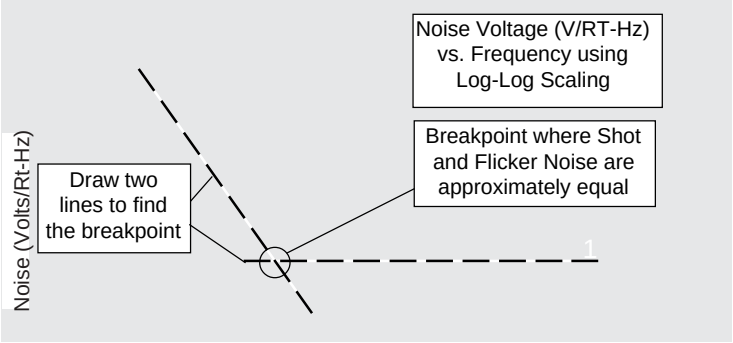
The equations governing shot and flicker noise are as follows:

$en^2 = 2 * q * ID + (KF * ID^{AF}/F)$ Diodes
$en^2 = 2 * q * I + (KF * I^{AF}/F)$ BJTs
$en^2 = 8 * k * T * gm/3 + (KF * ID^{AF}/F)$ JFETs and MOSFETs

where q is the charge of an electron, ID is the diode/drain current, I is the collector/base current, F is the frequency, k is Boltzman's constant, T is the temperature, and gm is the small signal transconductance.

At low frequencies the flicker noise will be dominant. At higher frequencies the shot noise will dominate and cause the noise response to become constant. If two lines are drawn, one corresponding to the slope of the noise curve at low frequen-

cies, and one corresponding to the final noise level at higher frequencies, they will intersect at a point called the breakpoint. This is the frequency where the shot noise and flicker noise are approximately equal. Then, using an assumed value for AF (normally 1), the equations listed above can then be solved for KF using the breakpoint frequency and noise voltage.

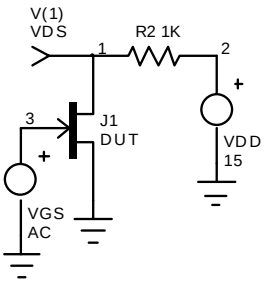


For example, using a breakpoint frequency of 1kHz, breakpoint voltage of 2nV, drain current of 10mA, and AF equal to 1 for a JFET (J105) we get:

$$8 * 1.38E\text{-}23 * 300 * .2/3 = KF * .01^{1}/1kHz$$
giving KF = 2.2E-16

The IsSpice4 .NOISE analysis can be used to produce the noise voltage associated with the device. The following circuit is setup for a JFET, but it can easily be adapted for any semiconductor. It will allow you to check the noise response produced by your model and the KF and AF values.

Noise Test Circuit




```
JFETNOIZ - Noise Test Circuit
.PRINT NOISE INOISE ONOISE
.AC DEC 10 10 100K
*Adjust Fstart and Fstop to match data sheet
.NOISE V(1) VGS DEC 10 10HZ 100KHZ
.PRINT AC  V(1)  VP(1)
VGS 3 0 AC 1 DC -5.9
VDD 2 0 15
R2 1 2 1K
*Adjust R, VGS, and VDD so (VDD - VDS)/R=ID from data sheet
J1 1 3 0 DUT
*Add device model with AF and KF parameters
.END
```

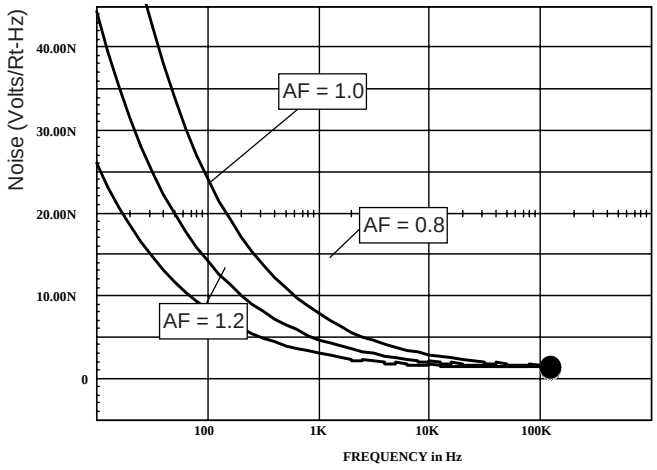
- Adjust VDD, VGS, and R so that (VDD - VDS) / R will give you the value of ID shown on the data sheet. VDS may also be found on the data sheet. Estimate the value of VGS from the family of curves which would give you the required VDS and ID needed to bias the circuit.

- Run the simulation and check the output file to verify the values for VDS and ID. If the value is off, tweak the value of VGS and repeat the simulation until VDS equals the data sheet specification and the value for the current, ID, is correct. Setting the correct bias and drain current flow is essential for the correct reproduction of shot noise.

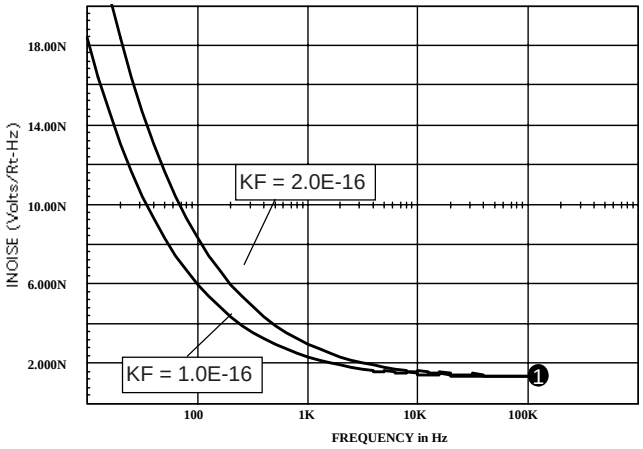
- When the correct bias has been achieved, run IntuScope and set the analysis type to Noise. Select and display the INOISE waveform. The equivalent input noise voltage in volts per root hertz will be displayed.

Tweaking AF And KF

AF controls the slope of the noise curve in the low frequency region where 1/f noise is dominant and normally varies from 0.5 to 2.0.

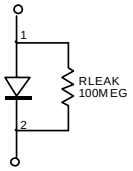


KF is a scalar multiplier for the flicker noise term. KF can be tweaked to adjust the overall magnitude and slope of the noise response in the low frequency region.



Diode Leakage

Diode leakage can be simulated by placing a large valued resistor (approximately 100 Meg Ohms) across the diode. This will also help to alleviate some convergence problems.



Schottky And Varactor Diodes

For Schottky Barrier diodes, the model parameter energy gap, EG, should be made .69, while the saturation temperature exponent, XTI, should be made 2.

Varactors, or voltage variable capacitors, are very similar to most pn junction diodes and can therefore be modeled by using a standard diode model containing only the CJO, VJ, and M model parameters. The process for finding the values for these parameters can be found in the “Calculating Charge Storage Parameters” section. You will need a graph of diode capacitance vs reverse voltage. If this graph is not available you will

not be able to generate an accurate model. Other diode parameters are not usually necessary. The varactor is normally reverse biased so the forward region parameters, N, IS, and RS are not needed. The device is not normally switched on and off so the transit time parameter is not critical. Also, the reverse voltage applied to the device should not be enough to break it down; therefore the reverse parameters BV and IBV are not needed.

Package Parasitics

Parasitics play an important part in the ViewAnalog simulation. Often they can dominate circuit performance. The addition of parasitics to your ViewAnalog simulation will depend upon your application and the frequency of operation. If you know that the design will be affected by parasitics, then they should be added. Otherwise, experimentation and testing of your design is encouraged to determine if parasitic elements are needed.

There are a number of parasitics that can be added to all basic ViewAnalog models and subcircuits. Parasitic capacitances can include the case capacitance, usually about .2-.3 pF, and the board capacitance which depends on several factors. You should review your data sheets and pcb layout and construction.

Lead inductance is due to the bonding wires inside the device package, as well as, the printed circuit board. Its addition is extremely important for high frequency devices.

In the best case, the only inductance will be from the device leads. This is usually in the range of 4nH to 10nH depending on the package. However, the inductance from the printed circuit card, including wiring to heatsink mounted devices and pc card interconnects, can increase inductance tenfold. Vendors will only provide information on the lead inductance. Measurements and a review of the pcb layout and construction should be able to provide accurate values for other pcb related parasitics.

Parasitic elements can be added externally to the SPICE element simply by adding the L or C to the appropriate terminal. This method will allow easy access to the parasitic value, but you will have to remember to add in the elements each time you use the device. Parasitics can be permanently added to a device that uses a subcircuit description by incorporating the parasitic elements directly into the subcircuit netlist. Devices utilizing a .MODEL statement may have to be combined with the parasitic elements into a subcircuit in order to combine them permanently.

Chapter 14 - Special Topics

Using Models Or Subcircuits With SPICE

The models and subcircuits created with SpiceMod may be used with any Berkeley SPICE 2 compatible program. The models and subcircuits use standard Berkeley SPICE 2G.6 model parameters and primitive elements.

After a model or subcircuit is saved to a file it may be cut and pasted into your SPICE input circuit netlist using any ASCII text editor. The netlist can then be simulated normally.

For example, to use a transistor model (model name = QN2222) created in SpiceMod, insert the following statements into your SPICE input netlist:

```
Q1 1 2 3 QN2222

.MODEL QN2222 NPN (IS=1.9E-14 BF=150 VAF=100 IKF=.175
+ISE=5E-11 NE=2.5 BR=7.5 VAR=6.38 IKR=.012 ISC=1.9E-13
+NC=1.2 RC=.4 XTB=1.5 CJE=26PF TF=.5E-9 CJC=11PF
+TR=30E-9 KF=3.2E-16 AF=1.0)
* 30 Volt .8 Amp 300 MHz SiNPN Transistor 08-19-1990
```

where Q1 is the SPICE reference designation calling a bipolar transistor, the numbers 1, 2, and 3 are the nodal connections to the collector, base, and emitter, and QN2222 is the model name referred to in the .MODEL statement. The .MODEL

statement can be copied from the file that SpiceMod places the model into.

To use a subcircuit created by SpiceMod, for example, a power MOSFET, insert the following statements into your SPICE input netlist:

```
X1 1 2 3 MTP15N06

.SUBCKT MP15N06E 10 20 40
*    TERMINALS:  D  G  S
*60 Volt 15 Amp 80M ohm N-Channel Power MOSFET 06-19-1992
M1   1  2  3  3  DMOS L=1U W=1U
RD  10  1  37M
RS  30  3  3M
RG  20  2  56
CGS  2  3  432P
EGD 12  0  2  1  1
VFB 14  0  0
FFB  2  1  VFB  1
CGD 13 14  549P
R1  13  0  1
D1  12 13  DLIM
DDG 15 14  DCGD
R2  12 15  1
D2  15  0  DLIM
DSD  3 10  DSUB
LS  30 40  7.5N
.MODEL DMOS NMOS (LEVEL=3 THETA=58M VMAX=125K
+ETA=2M VTO=3.1 KP=6.45)
.MODEL DCGD D (CJO=549P VJ=.6 M=.68)
.MODEL DSUB D (IS=62.2N N=1.5 RS=25.3M BV=60
+ CJO=838P VJ=.8 M=.42 TT=317N)
.MODEL DLIM D (IS=100U)
.ENDS
```

where X1 is the SPICE subcircuit call statement to the power MOSFET subcircuit and the .SUBCKT to the .ENDS statements are the subcircuit created by SpiceMod. The "*" comment statements at the top are optional and may be left out of your SPICE input netlist.

Appendices

Appendix A: Model References

For information on the models listed below please see the associated references. Technical papers are available directly from Intusoft. Other models are described in the IsSpice4 User's Guide and this manual. All Newsletters, numbered 1-34, are included in the Spice Applications Handbook (published by Intusoft). More recent newsletters can be obtained directly from Intusoft.

AM Generator (Signal.Lib) - Newsletter 32, Sept. 1993

Analog Switches (Hc.Lib) - Newsletter 25, June 1992

BiCMOS Models (Abtmbn.Lib) - Philips SPICE Modeling Series, "ABT and Multibyte™ Modeling Guide", April 1992

BJTs, Darlington (Bjtdar.Lib) - SpiceMod User's Guide

BJTs, Power (Powbjt.Lib) - SpiceMod User's Guide

Bridges (Cm2.Lib) - IsSpice4 User's Guide

Coax (Coax.Lib) - Newsletter 30, May 1993

Connectors (Conn.Lib/Conn2.Lib) - Newsletter 36/37, June/August 1994

Core Models (Device.Lib/Magnetic.Lib) - *Technical paper:* "Improved SPICE Model simulates Transformer's Physical Processes", L.G. Meares, C. Hymowitz, EDN August, 19 1993

Crosstalk Models (Device.Lib) - Newsletter 6, June 1987

Crystals with temperature effects (Device2.Lib) - Newsletter 16, Jan. 1990

Diodes, Photo (Diode5.Lib) - Newsletter 34, Jan. 1994

Diodes, Pin (RF.Lib) - Newsletter 31, July 1993

Diodes, Power Schottky (Diode5.Lib) - Newsletter 32, Sept. 1993

Diodes, Soft Recovery (Diode5.Lib) - Newsletter 32, Sept. 1993

Dual-Gate Mesfets (Dgmos.Lib) - Newsletter 22, August 1991

FAST Models (Abtmbn.Lib) - Philips SPICE Modeling Series, "Design Guide for SPICE Simulation of Philips Bipolar Logic", March 1990

Fuses (Thermal.Lib) - Newsletter 21, April 1991

Fuzzy Logic (Fuzzy.Lib) - Newsletter 28, January 1993

ECL (Ecl.Lib) - Newsletter 36, June 1994

Ground Plane (Device.Lib) - Newsletter 6, June 1987

Hall Sensors (Hsensor.Lib) - Newsletter 33, November 1993

IBIS Models (Ibis1.Lib) - Newsletter 30/31, May/July 1993

IGBTs (Igbt.Lib) - Newsletter 25, June 1992, SPICEMOD User's Guide, *Technical paper:* "A SPICE Model for IGBTs", Charles Hymowitz, APEC 1995

Laplace Models (Sys.Lib, CM1.Lib, Scn.Lib) - Newsletter 19, March 1990 (SC Filters), Newsletter 19/28, Oct. 1990/Jan 1993 (Pole-Zero functions), Newsletter 39, Nov. 1994 (Laplace expressions)

Lasers (Diode.Lib) - Newsletter 14, July 1989

Mechanical Models (Mech.Lib) - Newsletter 19/20, Oct. 1990/Jan. 1991

Mosfets, Power (Powmos.Lib) - Newsletter 27, Nov. 1992, SPICEMOD User's Guide

Movs (Mov.Lib) - EDN Design Idea, "MOV Model Spoofs SPICE", Jim Honea, 3/28/91, pg. 35

Neural Networks (Neural.Lib) - Newsletter 13/14, April/July 1989

NTSC Generator (Signal2.Lib) - Newsletter 40, June 1995

Platinum Thermal Resistor (Device2.Lib) - Newsletter 24, Feb. 1992

PSK/FSK Generators (Signal2.Lib) - Newsletter 37, August 1994

Pressure Sensors (Psensor.Lib) - Newsletter 33, November 1993

PWM IC Models (Pwm.Lib) - "Circuit Simulation of Switching Regulators With Spice2", Dr. Vince Bello, Norden Systems, Norwalk CT 06856, 1994

RF Beads (RF.Lib) - Newsletter 23, Nov. 1991

SCR (Scr.Lib) - Newsletter 24, Feb. 1992, SPICEMOD User's Guide

Switched Capacitor Elements & Filters (Scn.Lib) - Newsletter 4, March 1987, Newsletter 17, March 1990

Test Generators (Signal2.Lib) - Newsletter 39, Nov. 1994

Thermistors (Thermal.Lib) - Newsletter 11, Oct. 1988

Time Dependent Elements (Device.Lib) - Paper

Tungsten Lamp (Thermal.Lib) - Newsletter 11, Oct. 1988

Transformer, Single/Center-Tap (Device.Lib) - Newsletter 12, Feb. 1989

Transimpedance Opamps (Nonlin.Lib) - Newsletter 15, Sept. 1989

Vacuum Tubes, Simple polynomial based models (Vacuum.Lib) - Newsletter 12, Feb. 1989

Vacuum Tubes, Complex B element based models (Vacuum.Lib) - Newsletter 34/35, Feb./April 1994

Variable Phase Generators (Signal2.Lib) - Newsletter 33, November 1993

Wire Models (Device.Lib) - Newsletter 6, June 1987

Z transform Elements (Sys.Lib/Scn.Lib) - Newsletter 4, Feb. 1987, Newsletter 17, March 1990

Appendix A: Model References

Index

D

E

J

K

L

M

N

O

P

Q

R

S

T

U

V

W

X

Z